

FIG. 1a

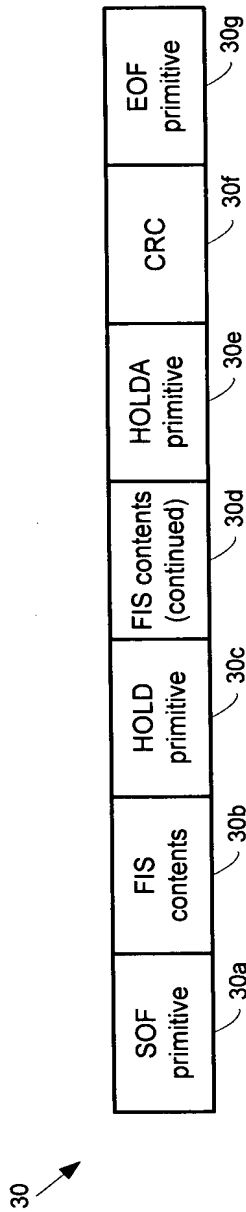


FIG. 1b

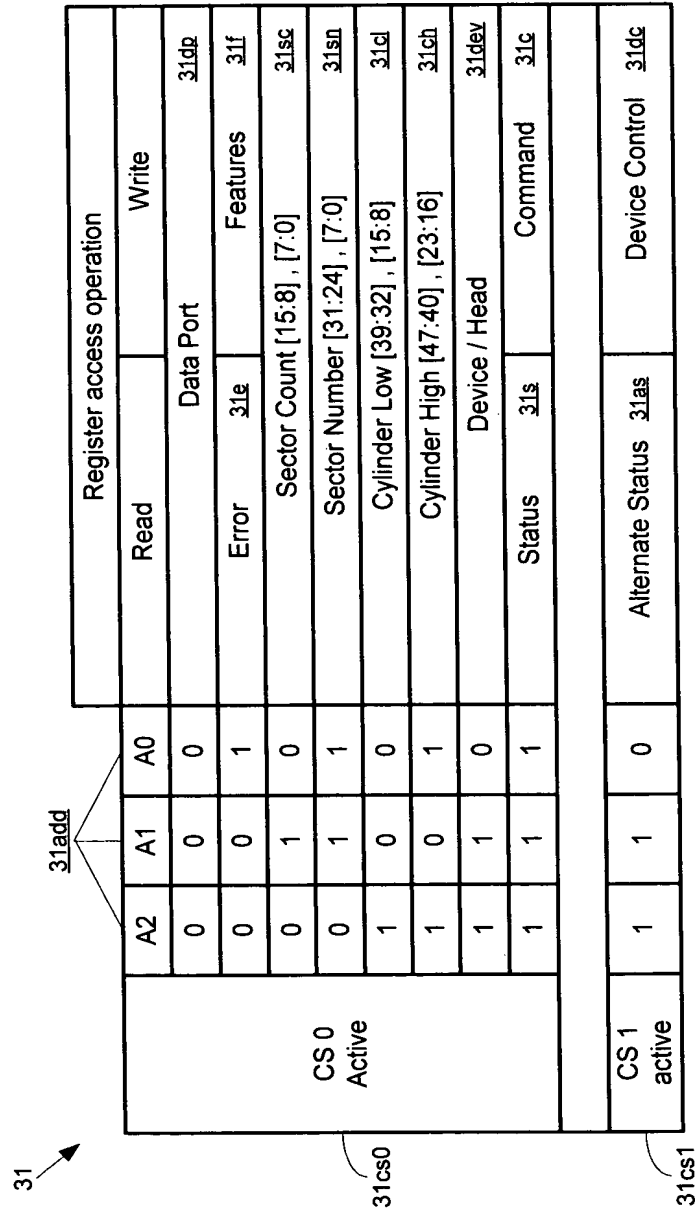


FIG. 1c

3/43

0	Features	Command	C	R	R	Reserved (0)	FIS Type (27h)
1	Dev / Head	Cyl High				Cyl Low	Sector Number
2	Features (exp)	Cyl High (exp)				Cyl Low (exp)	Sector Num (exp)
3	Control	Reserved (0)				Sector Count (exp)	Sector Count
4	Reserved (0)	Reserved (0)				Reserved (0)	Reserved (0)

40(i)

FIG. 1d(i) Register FIS Host to Device

0	Reserved (0)	Reserved (0)	R	R	R	Reserved (0)	FIS Type (39h)
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40(iii)

FIG. 1d(iii) DMA Activate FIS, Device to Host

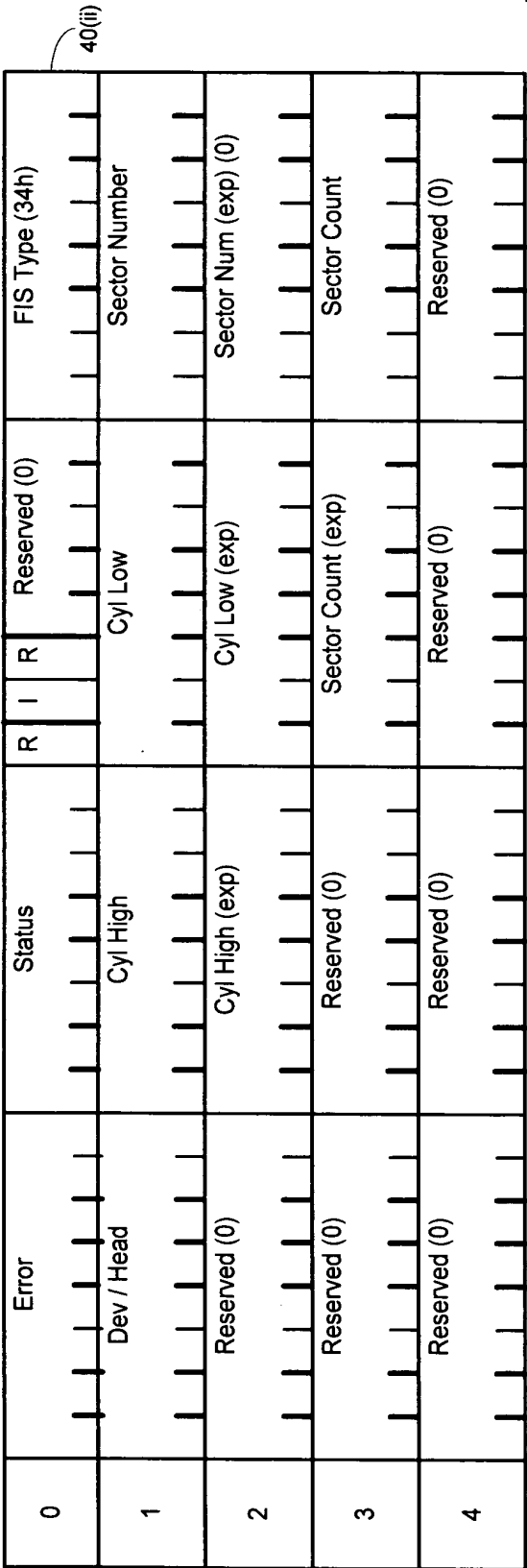


FIG. 1d(ii) Register FIS Device to Host

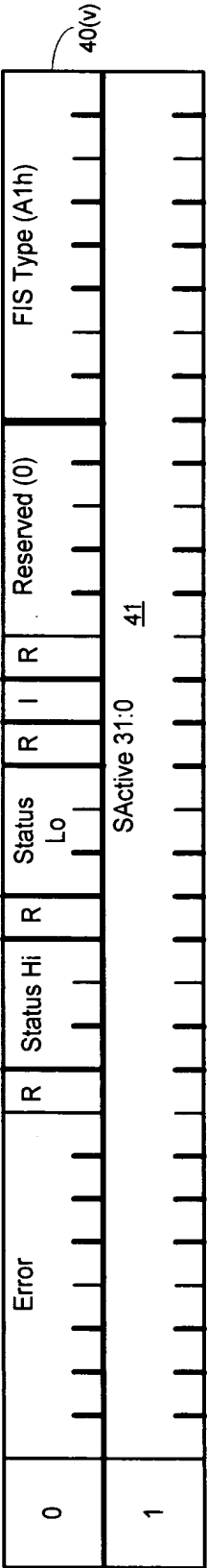


FIG. 1d(v) Set Device Bits FIS

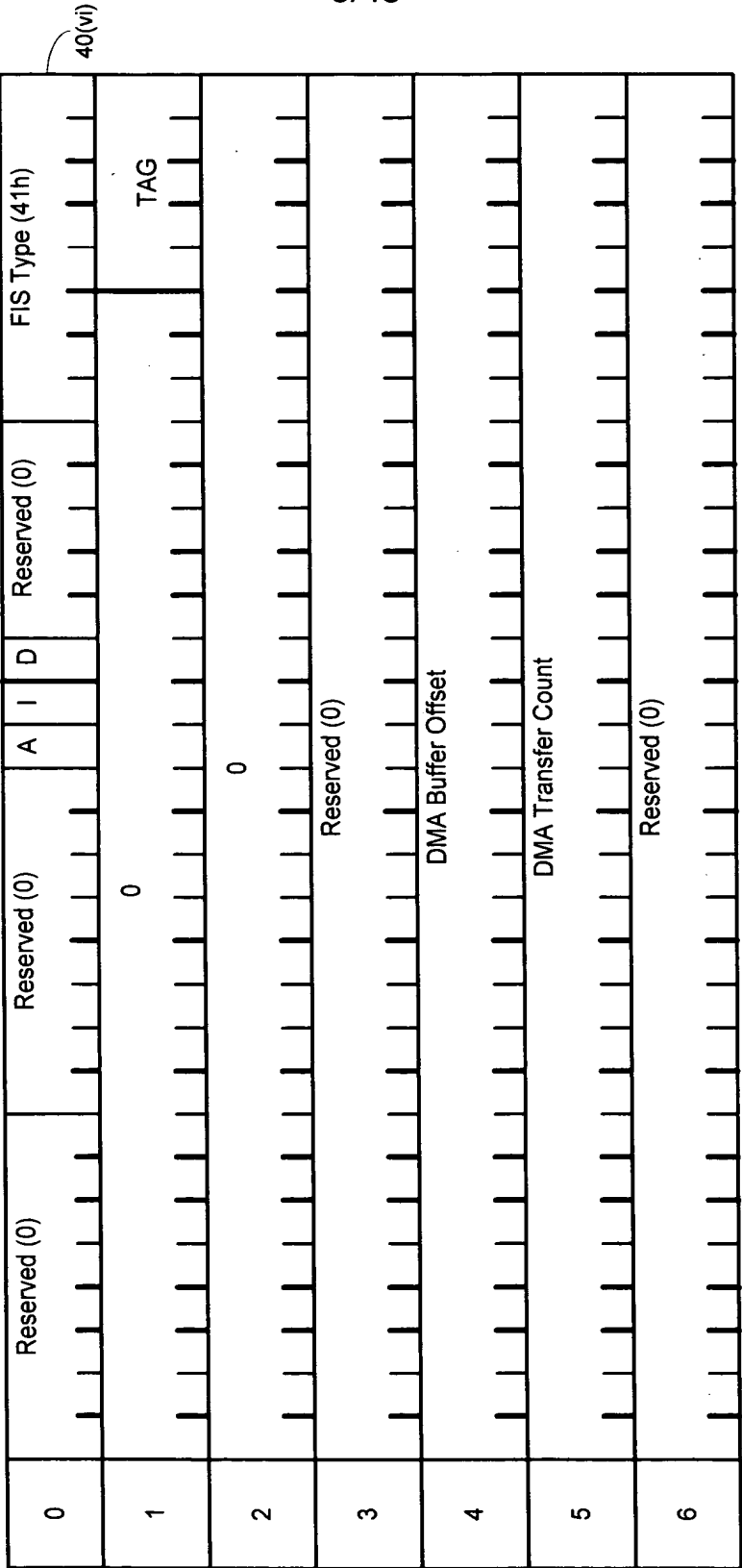


FIG. 1d(iv) DMA Setup FIS

6/43

0	Error	Status	R	I	D	Reserved (0)	FIS Type (5Fh)
1	Dev / Head	Cyl High	Cyl Low			Sector Number	
2	Reserved (0)	Cyl High (exp)	Cyl Low (exp)			Sector Number (exp) (0)	
3	E_Status	Reserved (0)	Sector Count (exp)			Sector Count	
4	Reserved (0)		Transfer Count				

FIG. 1d (vi) PIO Setup FIS

0	Reserved (0)	Reserved (0)	R	R	R	Reserved (0)	FIS Type (46h)
...	N Dwords of data (minimum of one Dword - maximum of 2048 Dwords)						
...							
n							

FIG. 1d(vii) Data FIS

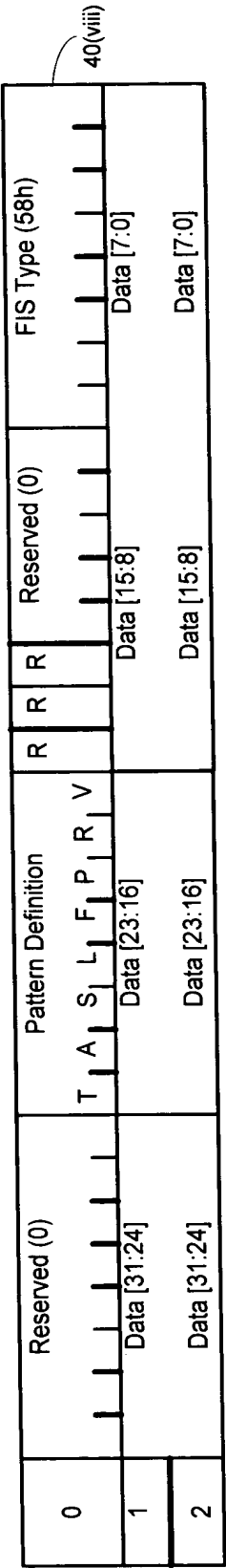


FIG. 1d (viii) BIST Activate FIS

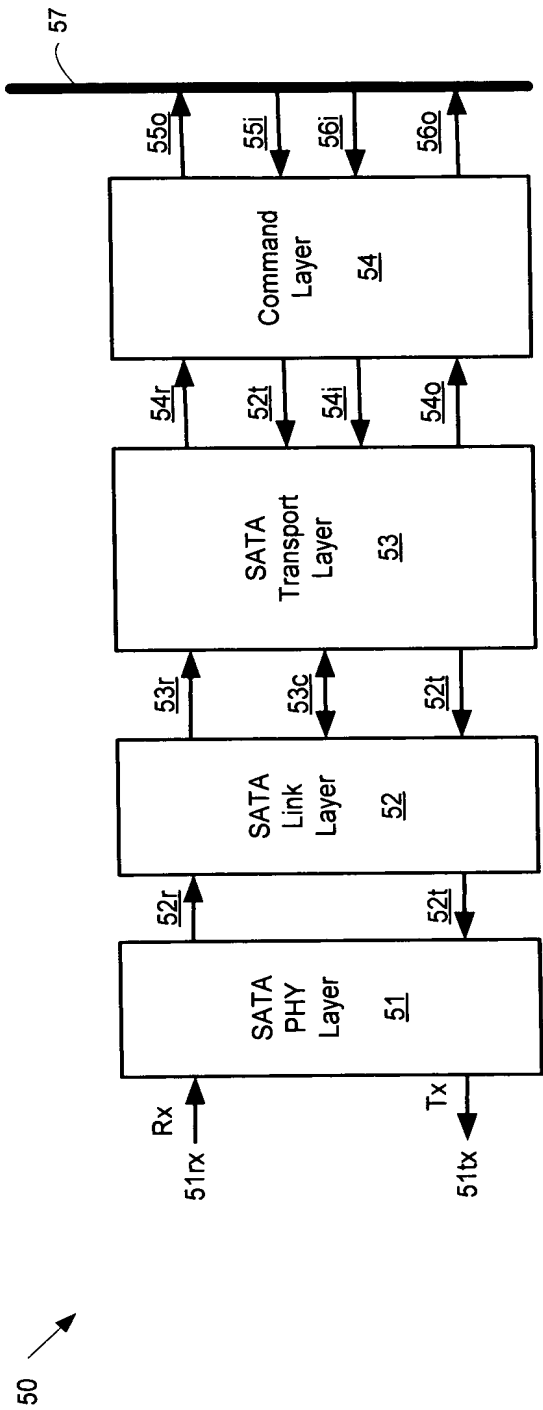


FIG. 2a

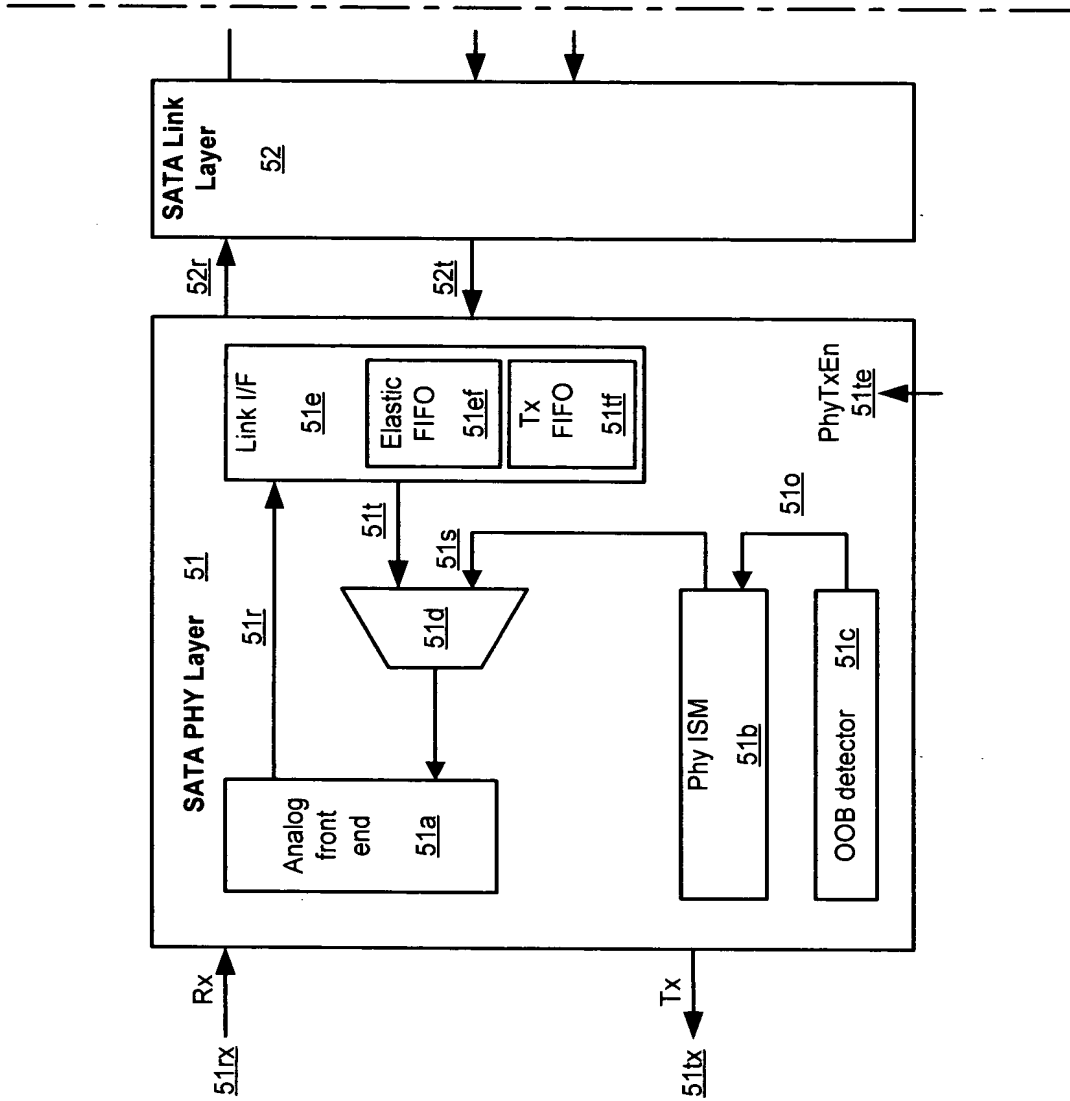


FIG. 2b(i)

Fig. 2b(i)	Fig. 2b(ii)
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Key To
 FIG. 2b

50

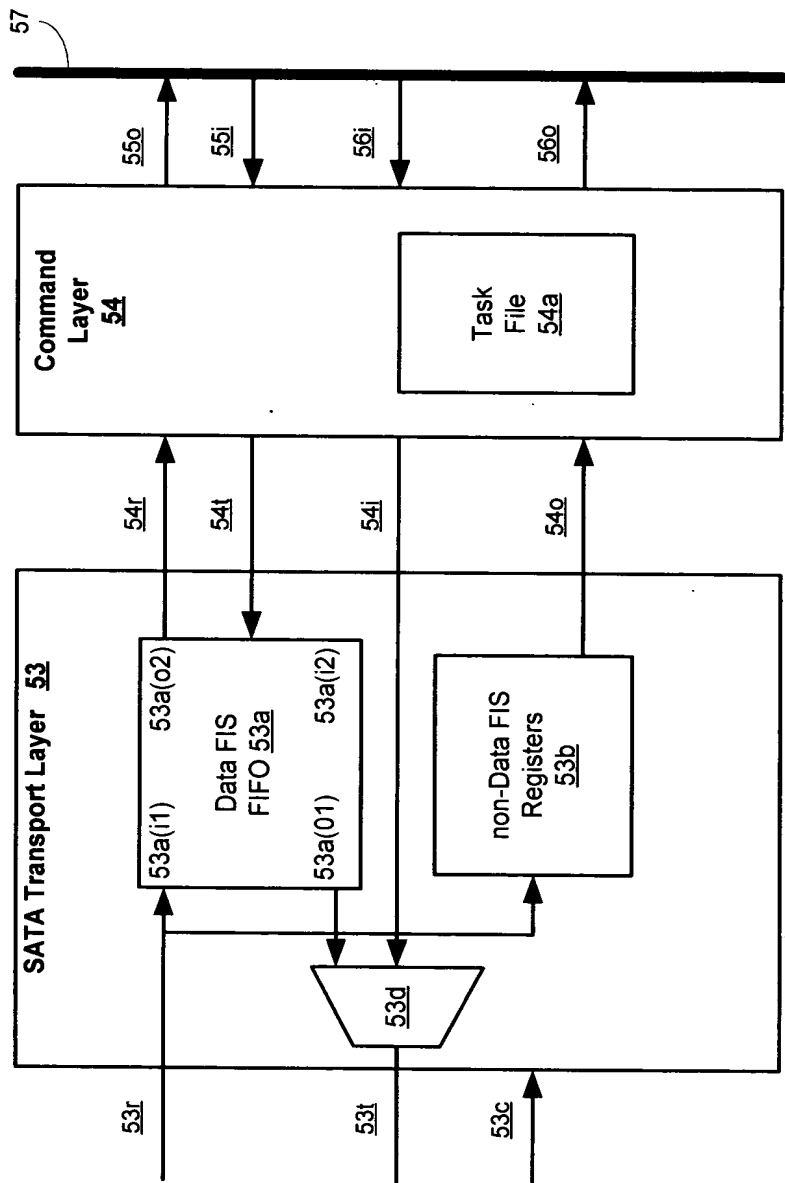


FIG. 2b(ii)

10/43

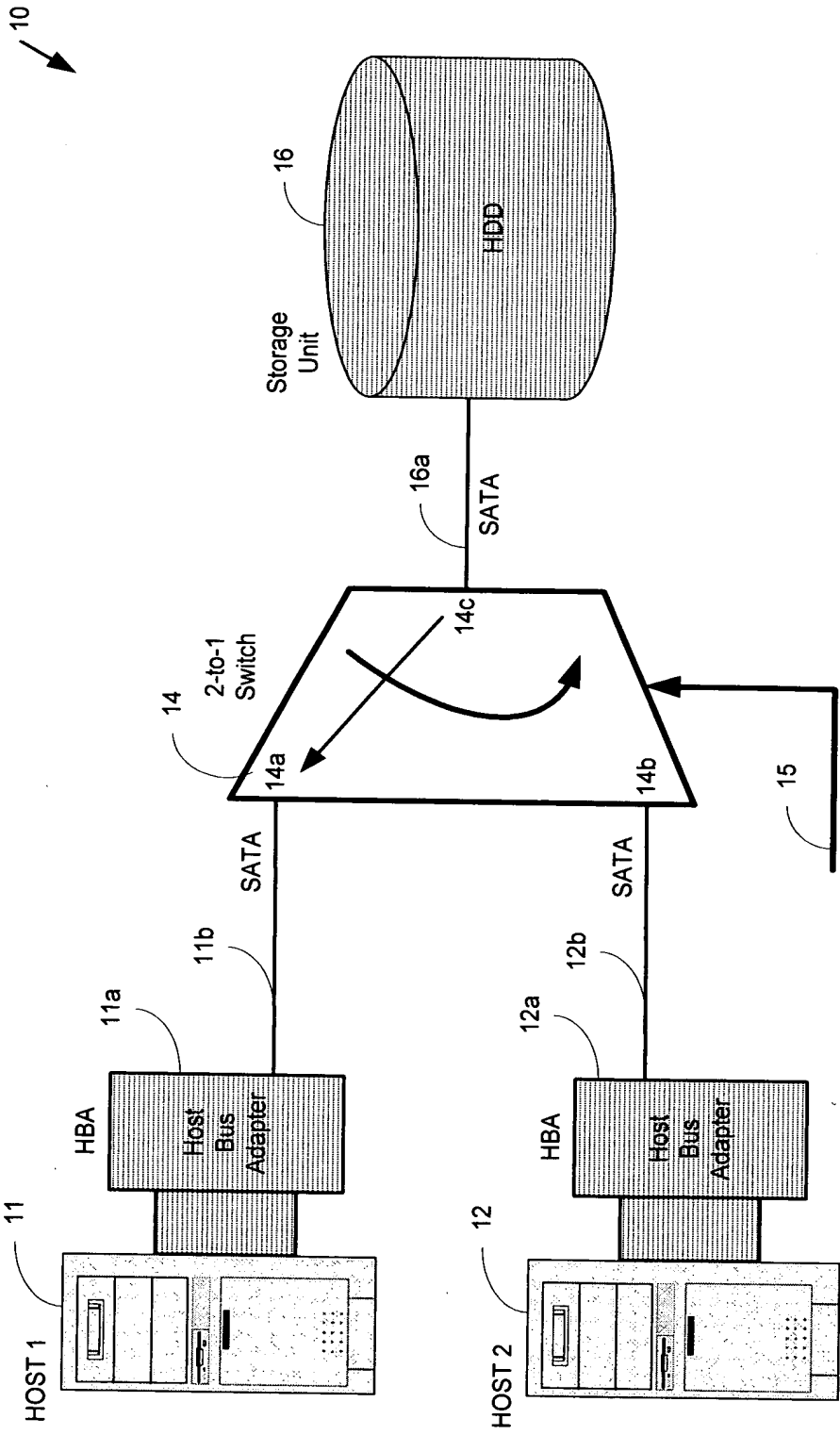


FIG. 3a

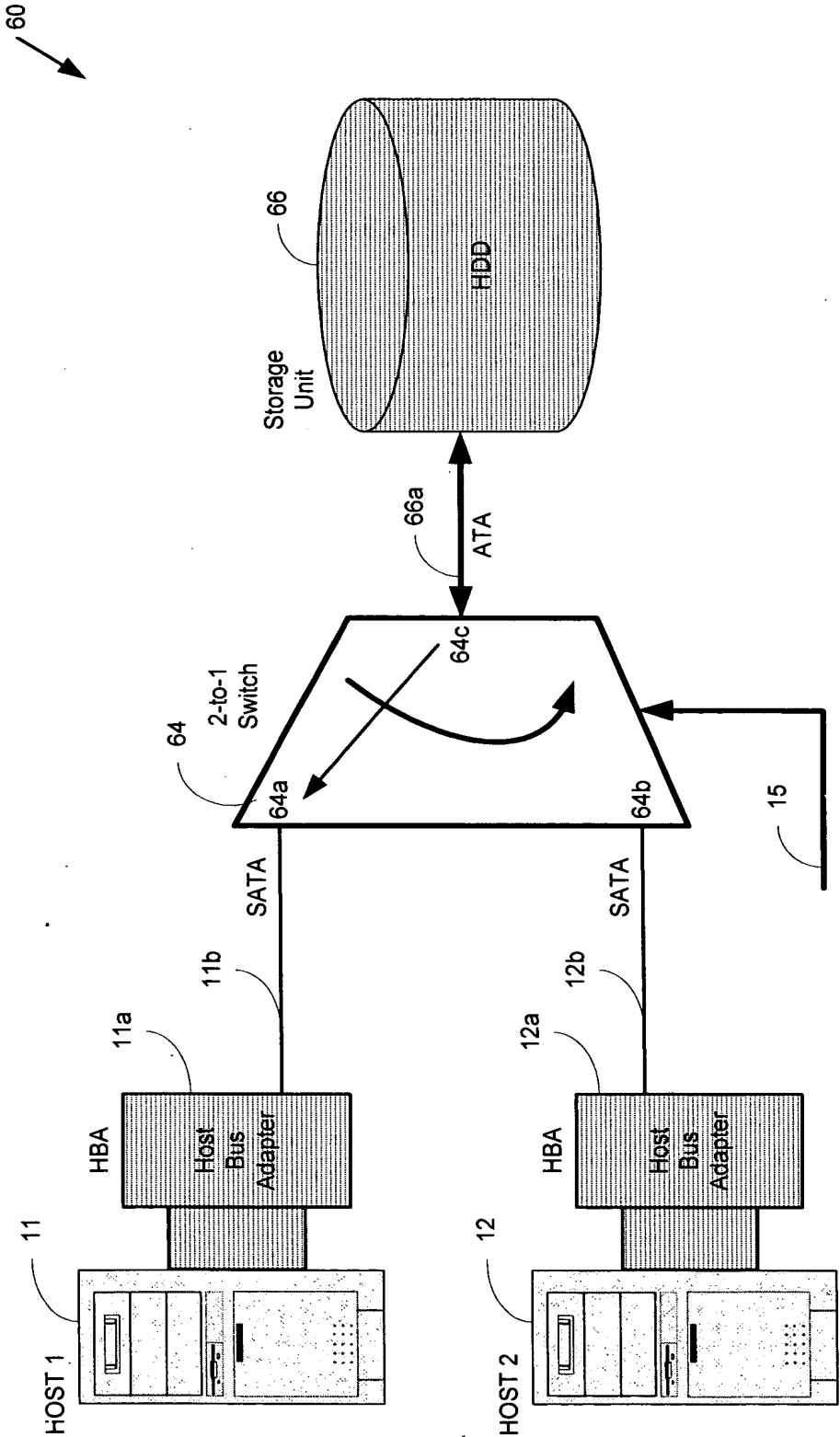


FIG. 3b

FIG. 4a FIG. 4b

Key To
 FIG. 4

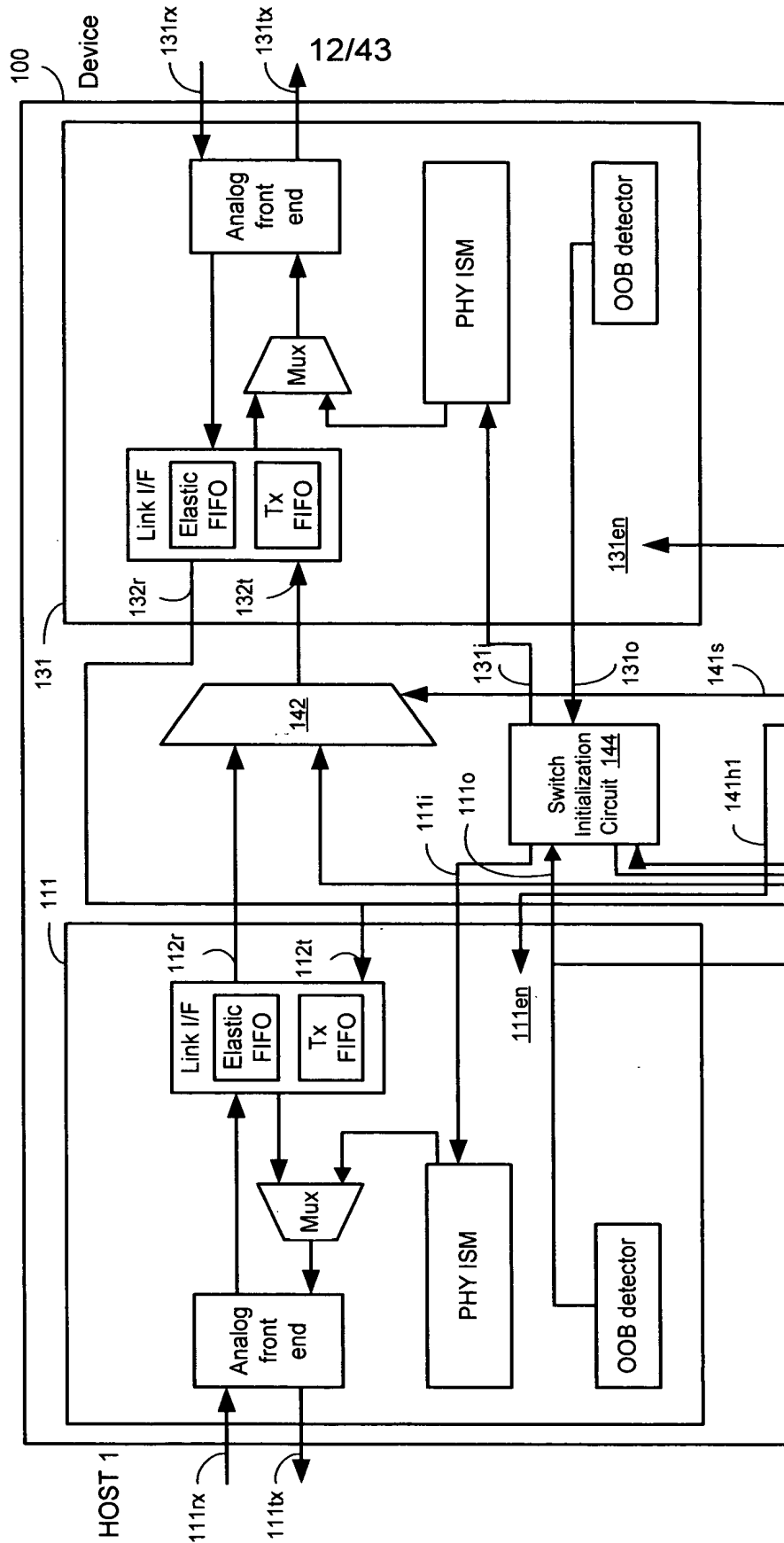


FIG. 4a

13/43

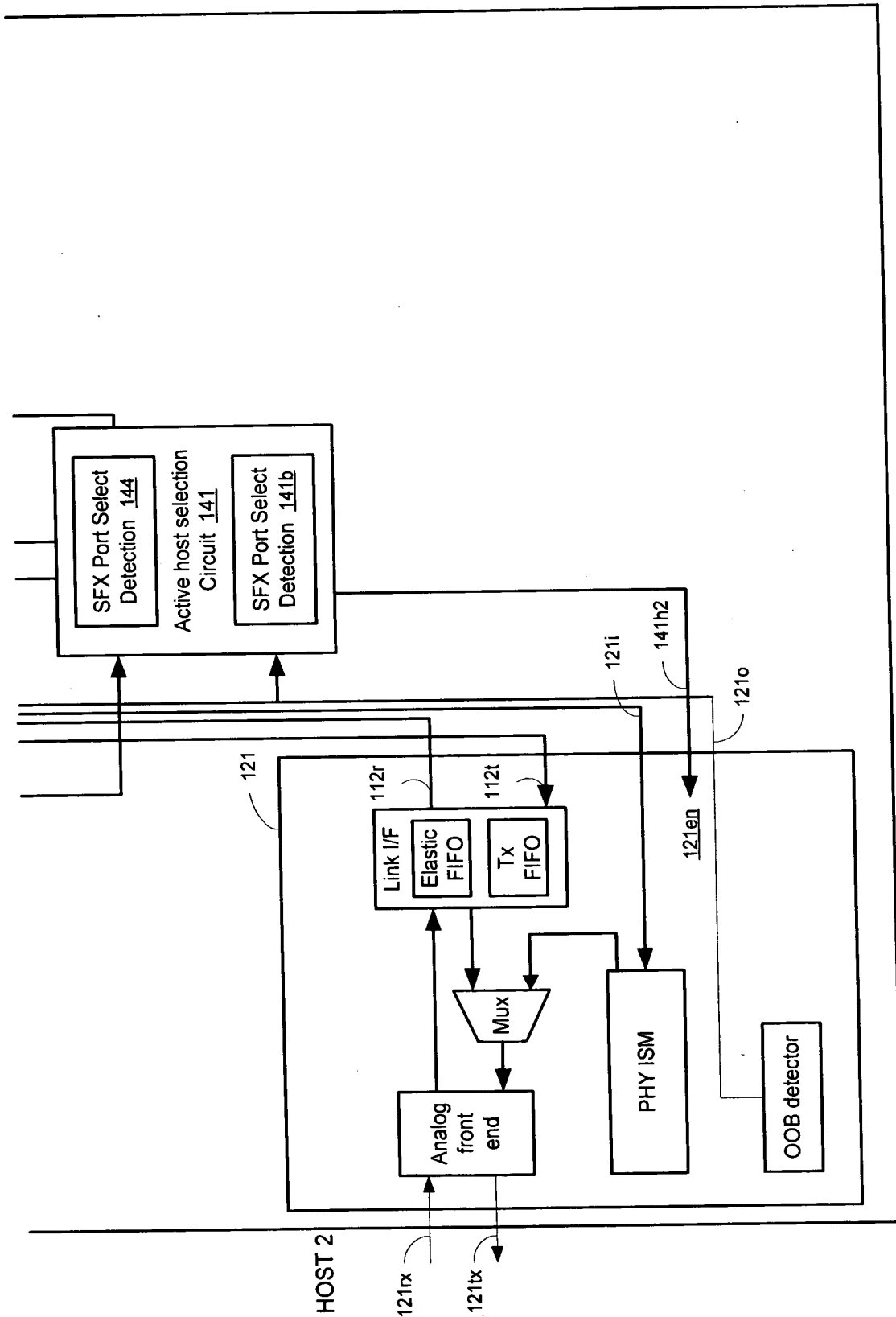


FIG. 4b

14/43

FIG. 5a	FIG. 5b
FIG. 5c	Key To FIG. 5

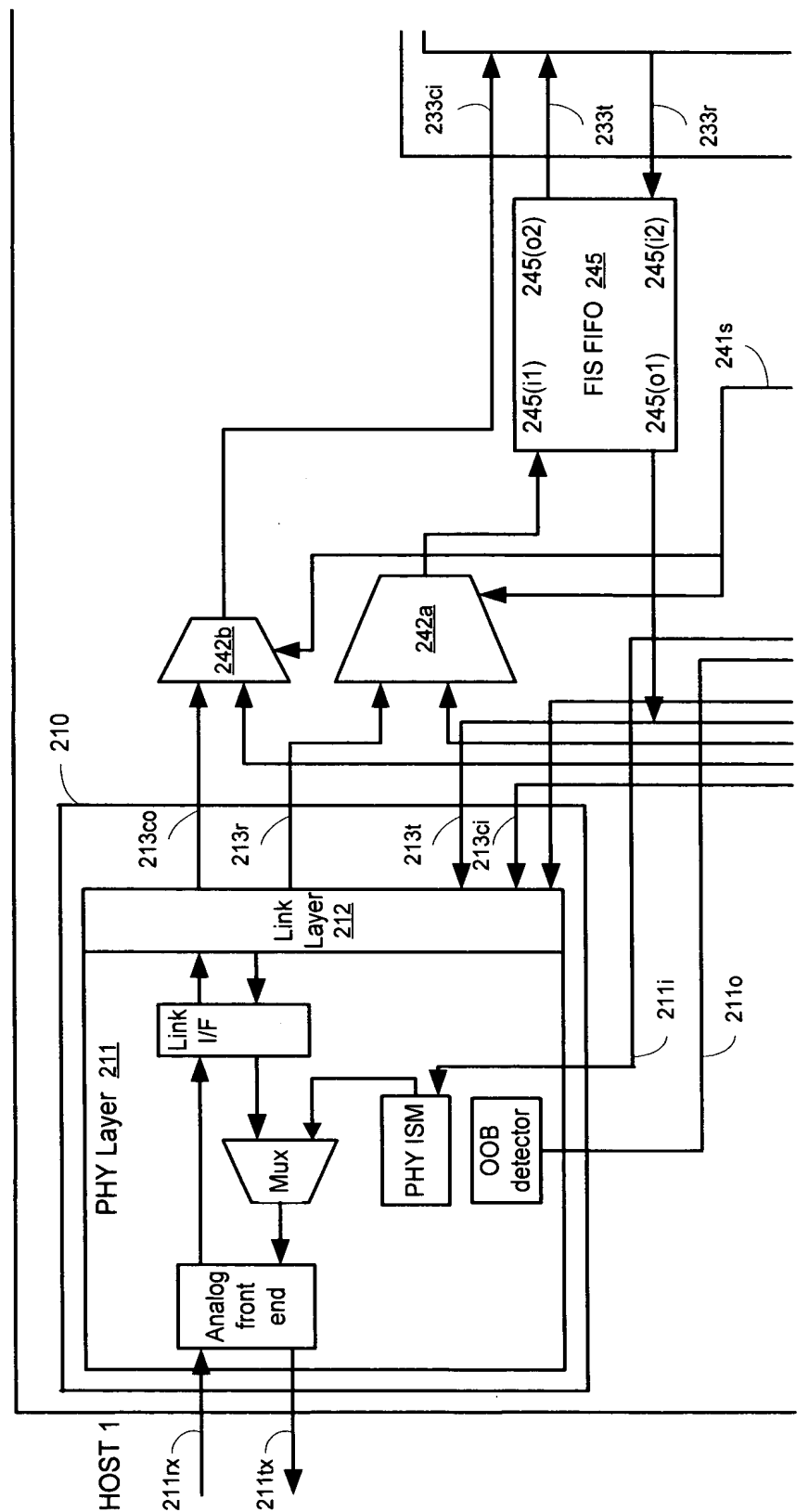


FIG. 5a

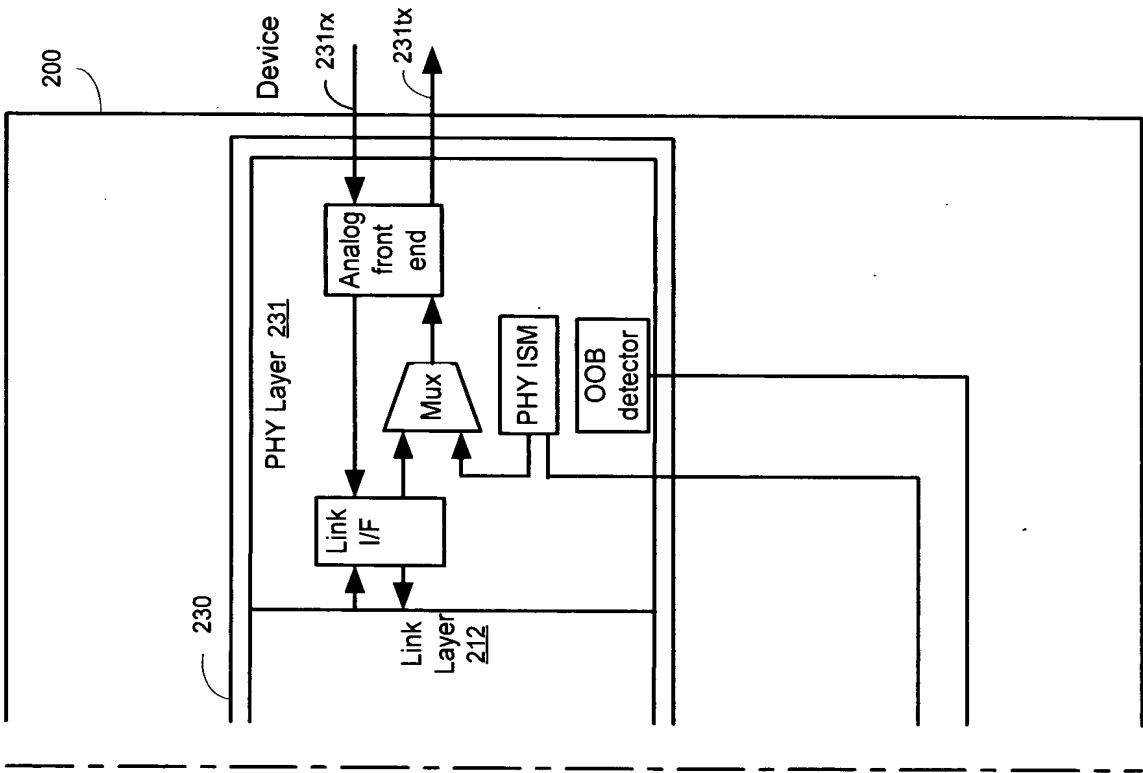


FIG. 5b

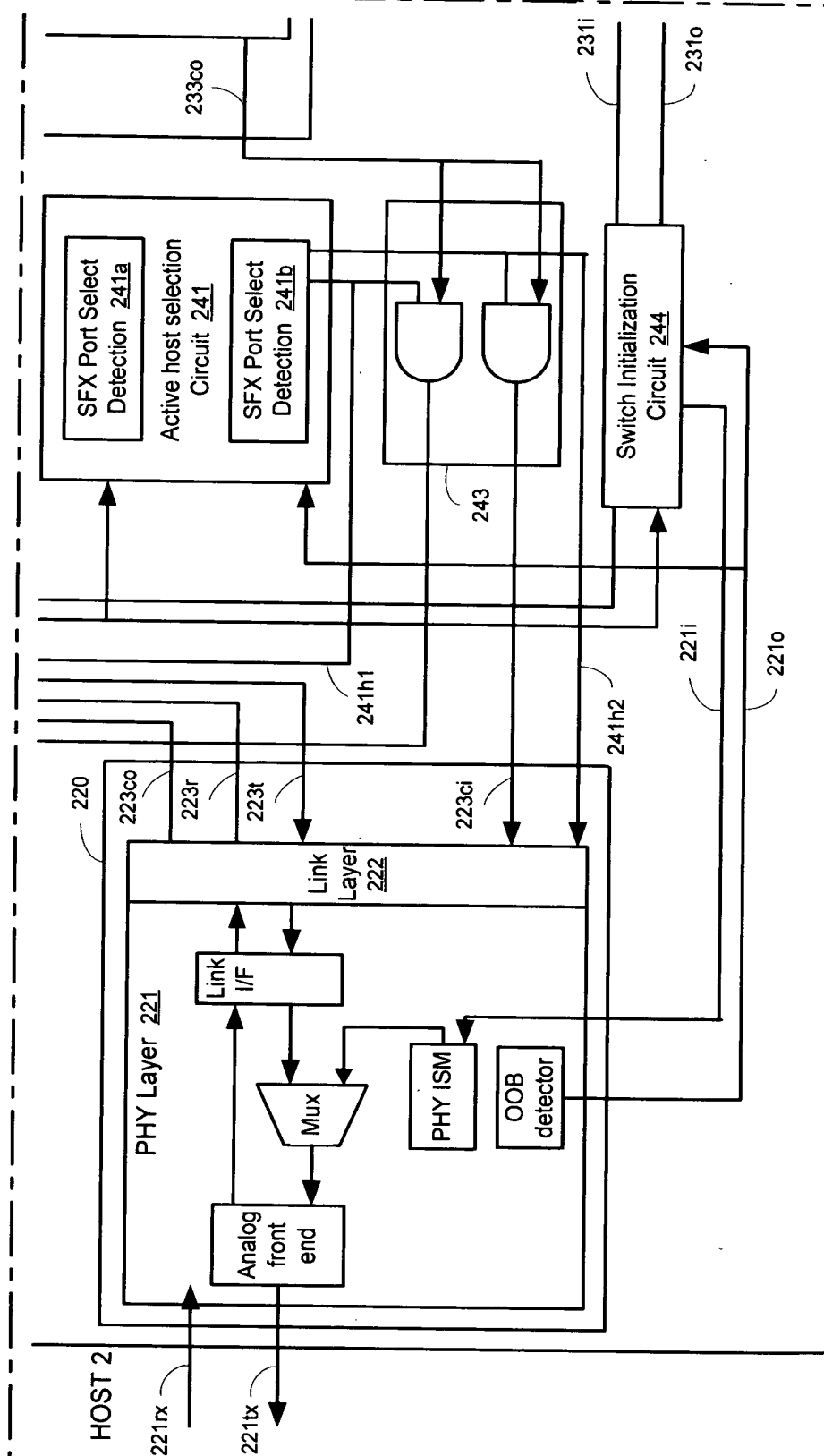


FIG. 6a	FIG. 6b
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Key To
FIG. 6

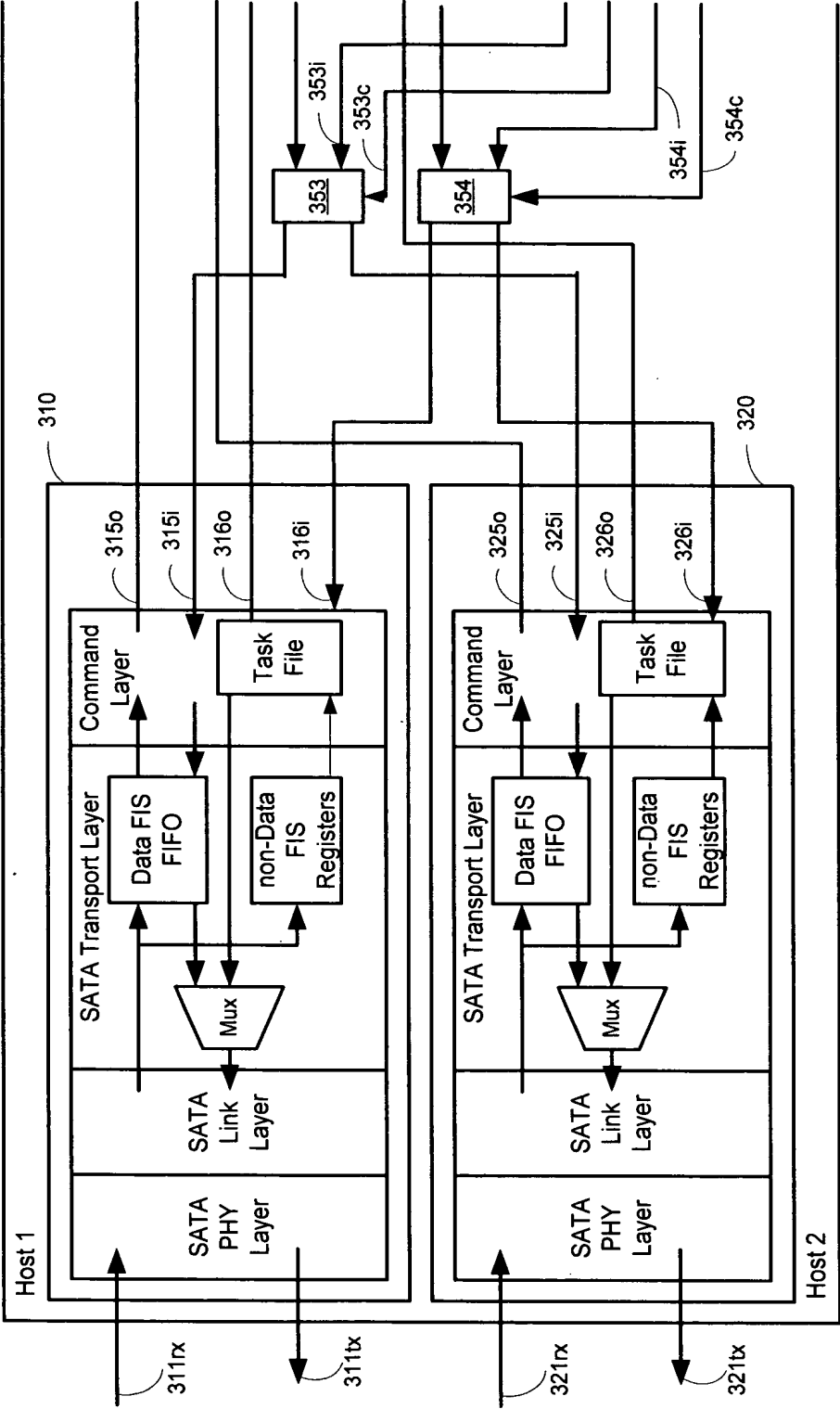


FIG. 6a

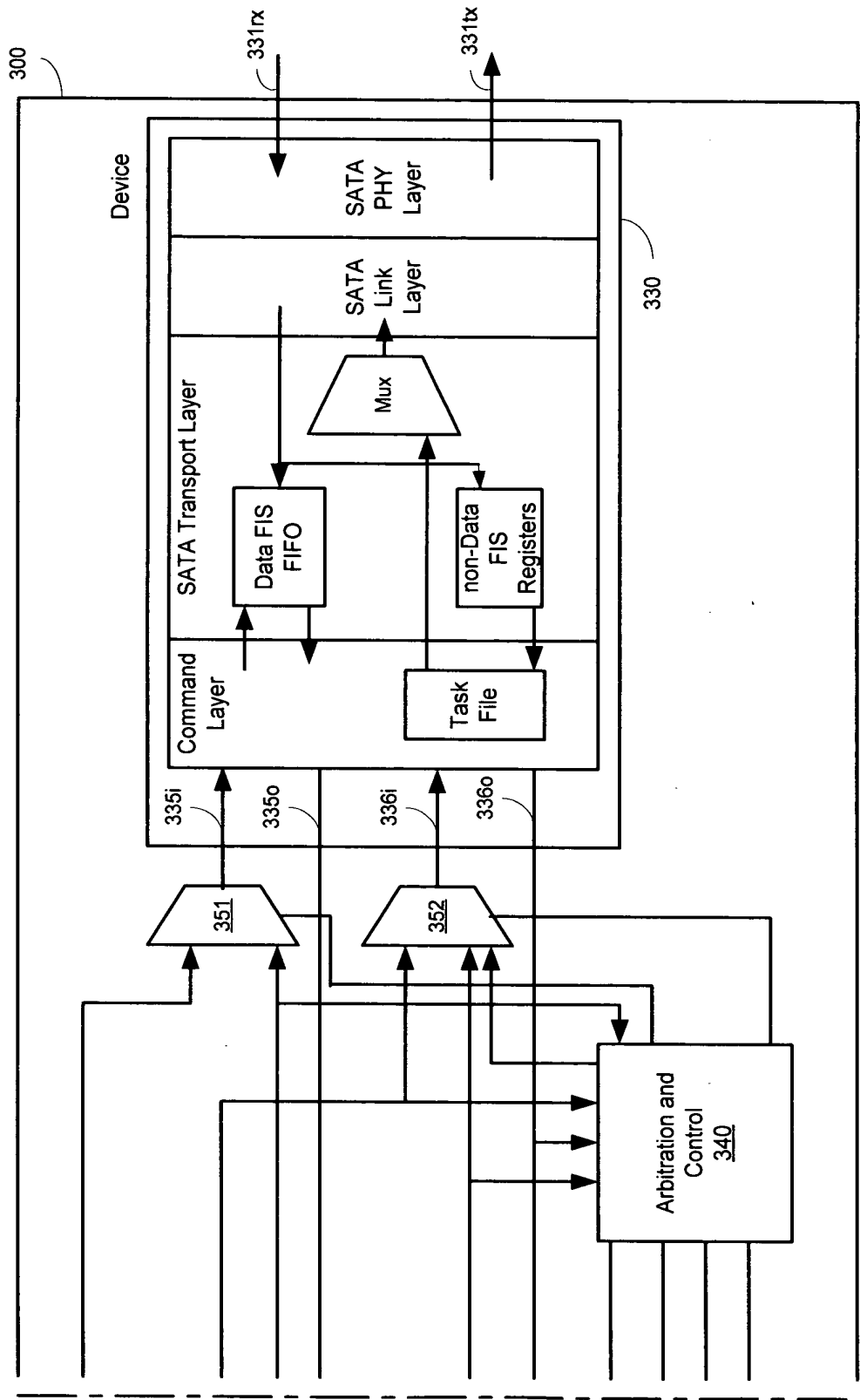


FIG. 6b

19/43

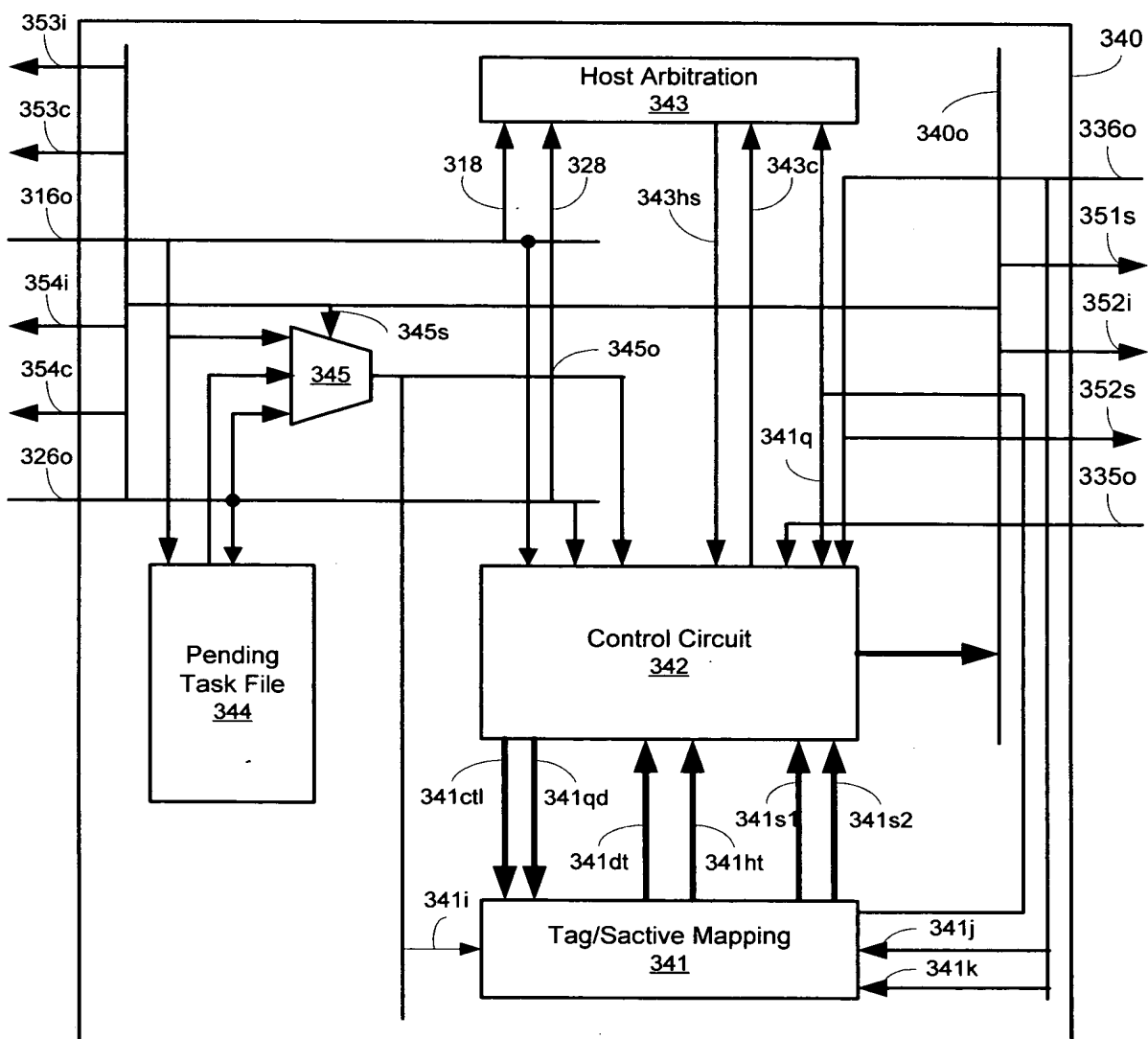


FIG. 7a

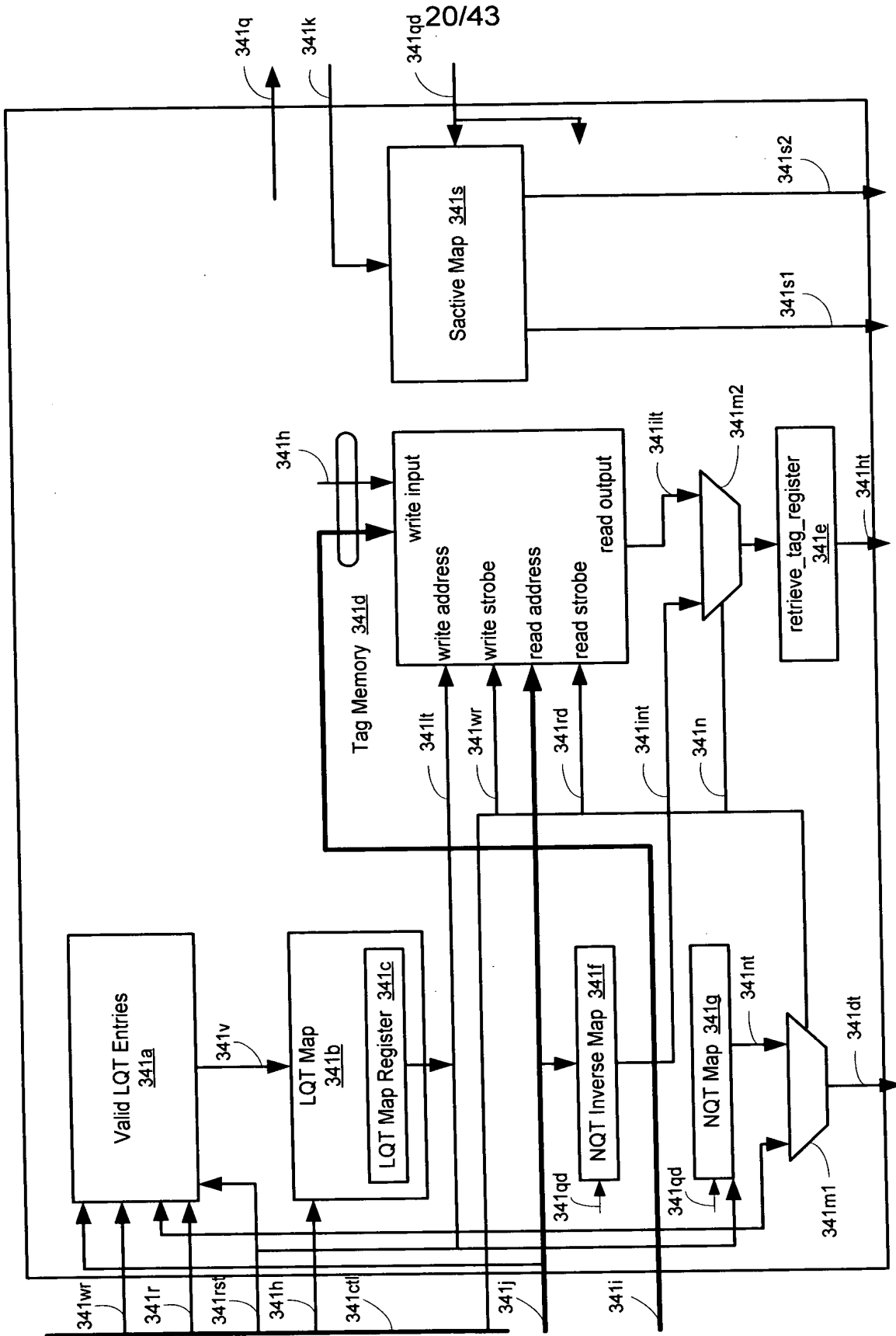


FIG. 7b

21/43

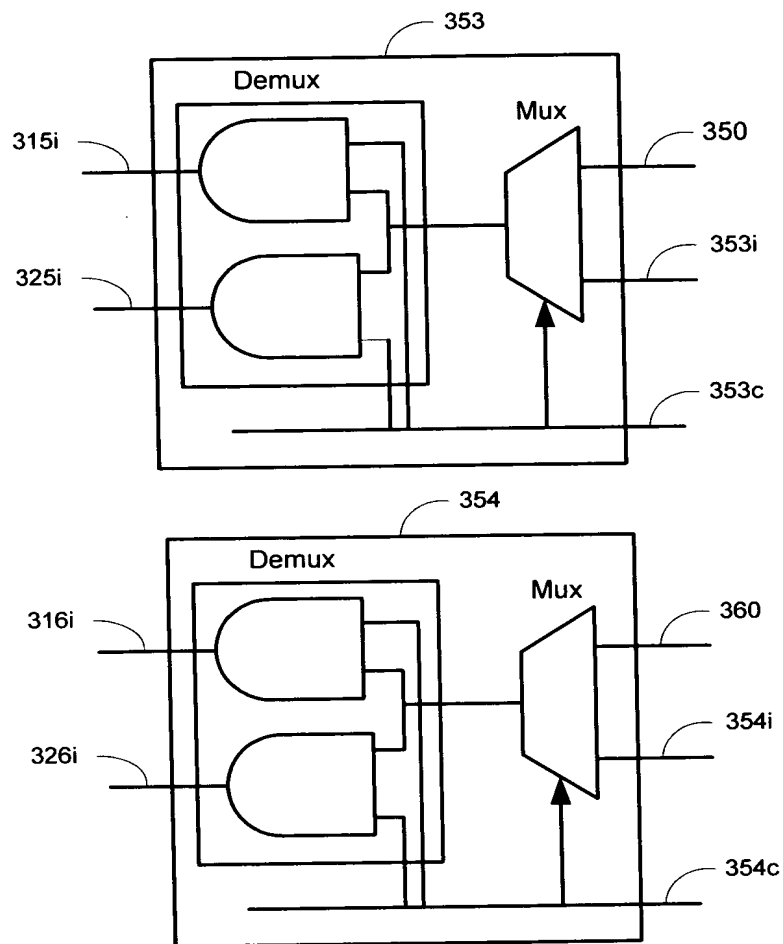


FIG. 7c

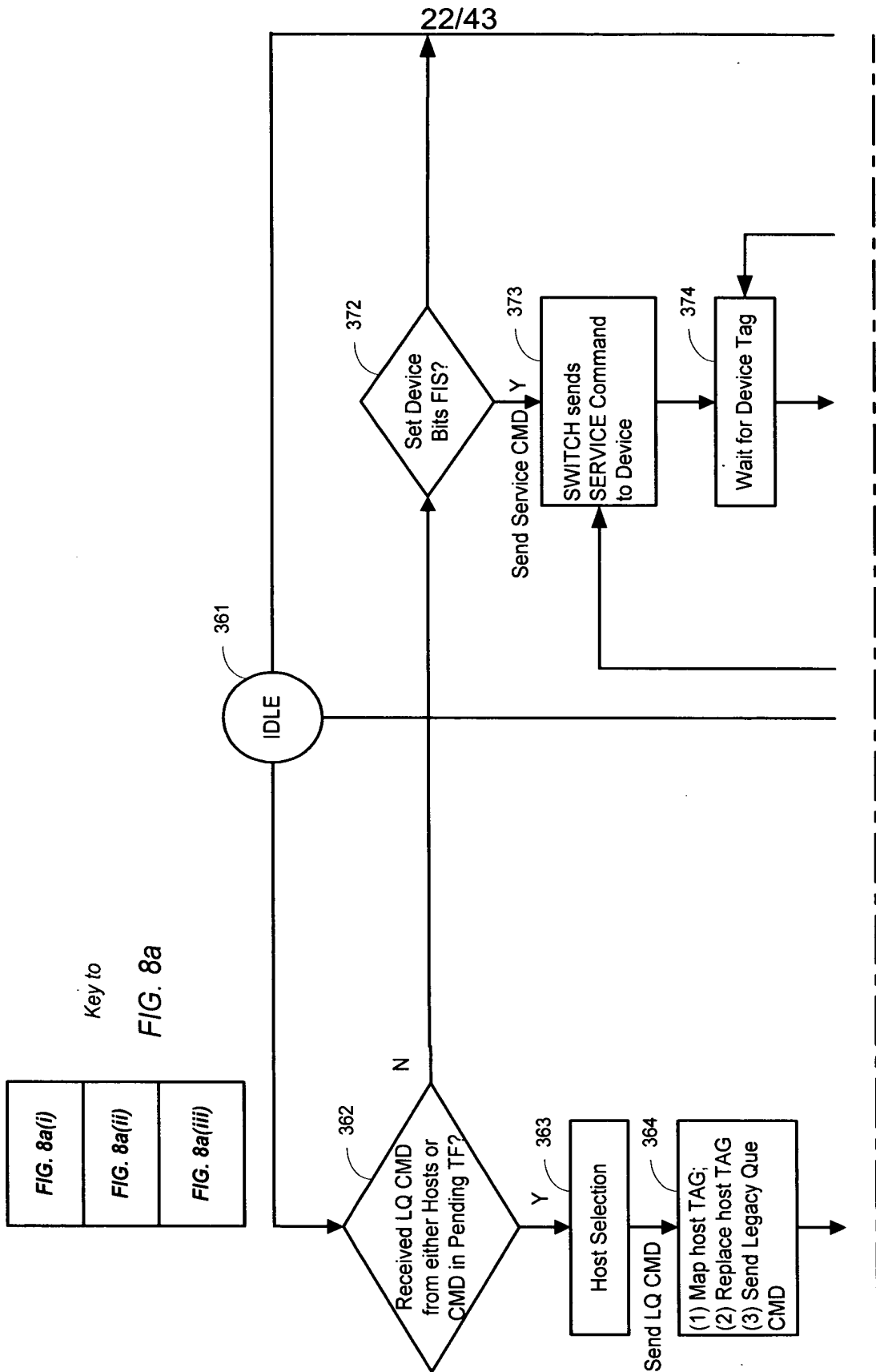


FIG. 8a(i)

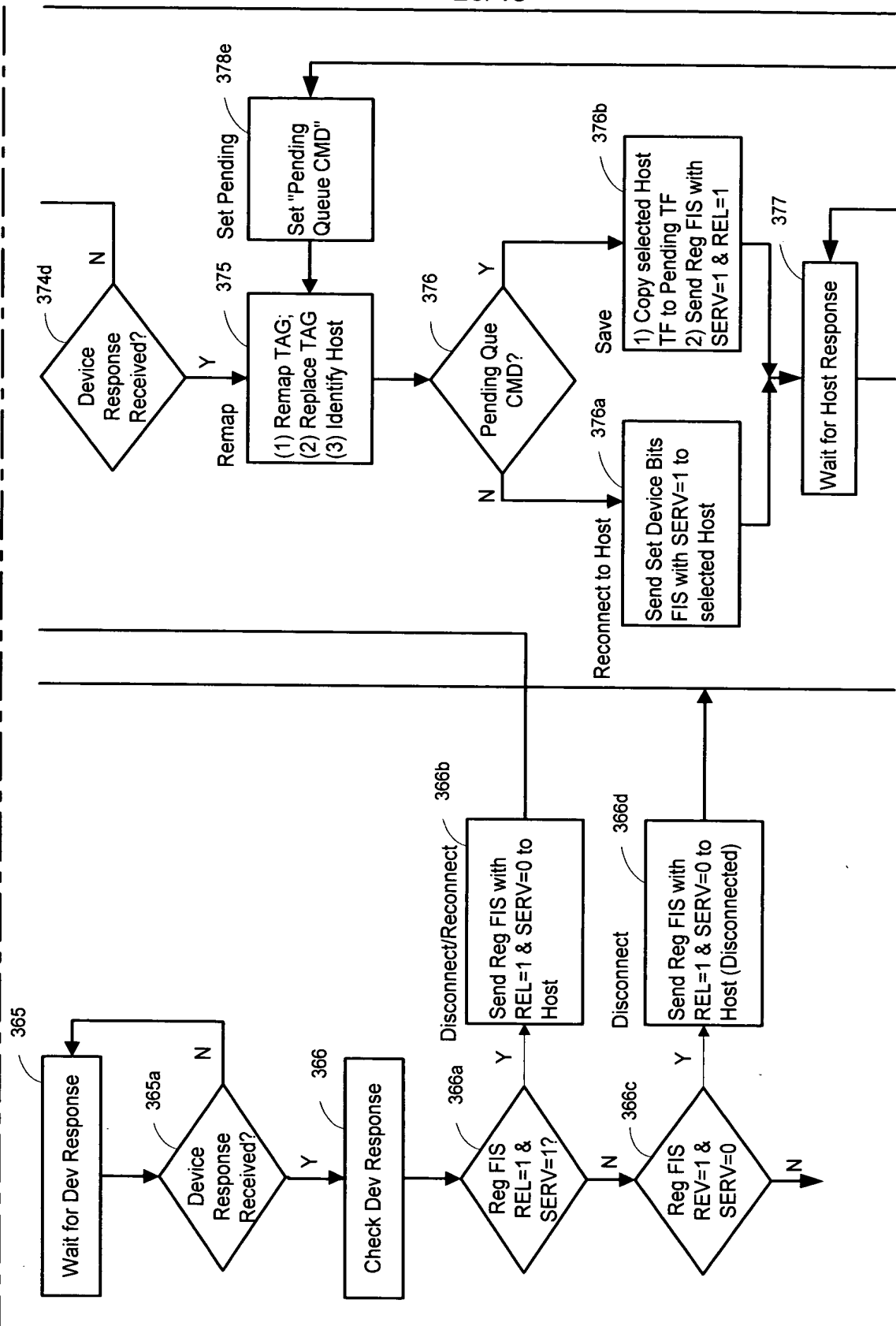


FIG. 8a(ii)

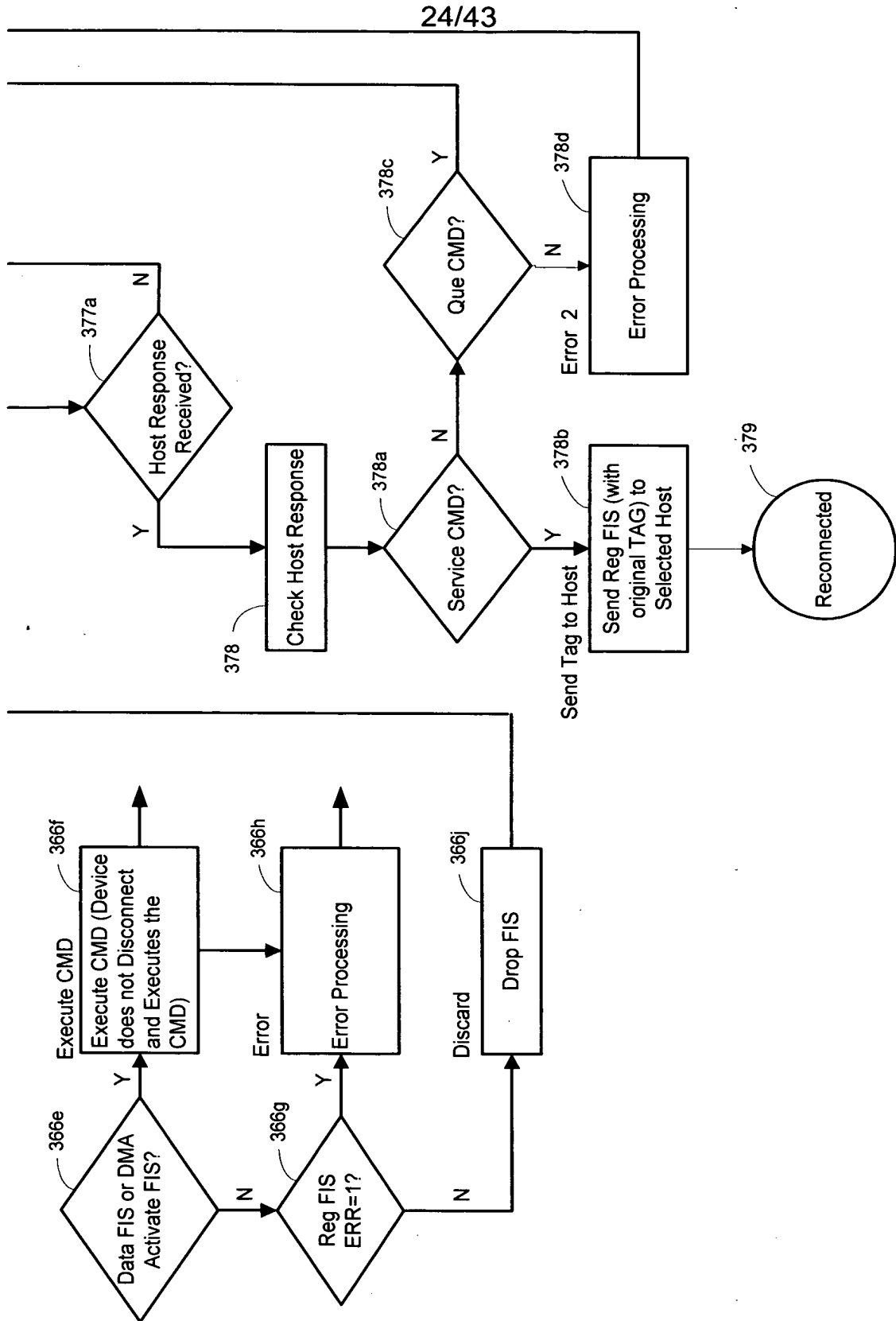


FIG. 8a(iii)

25/43

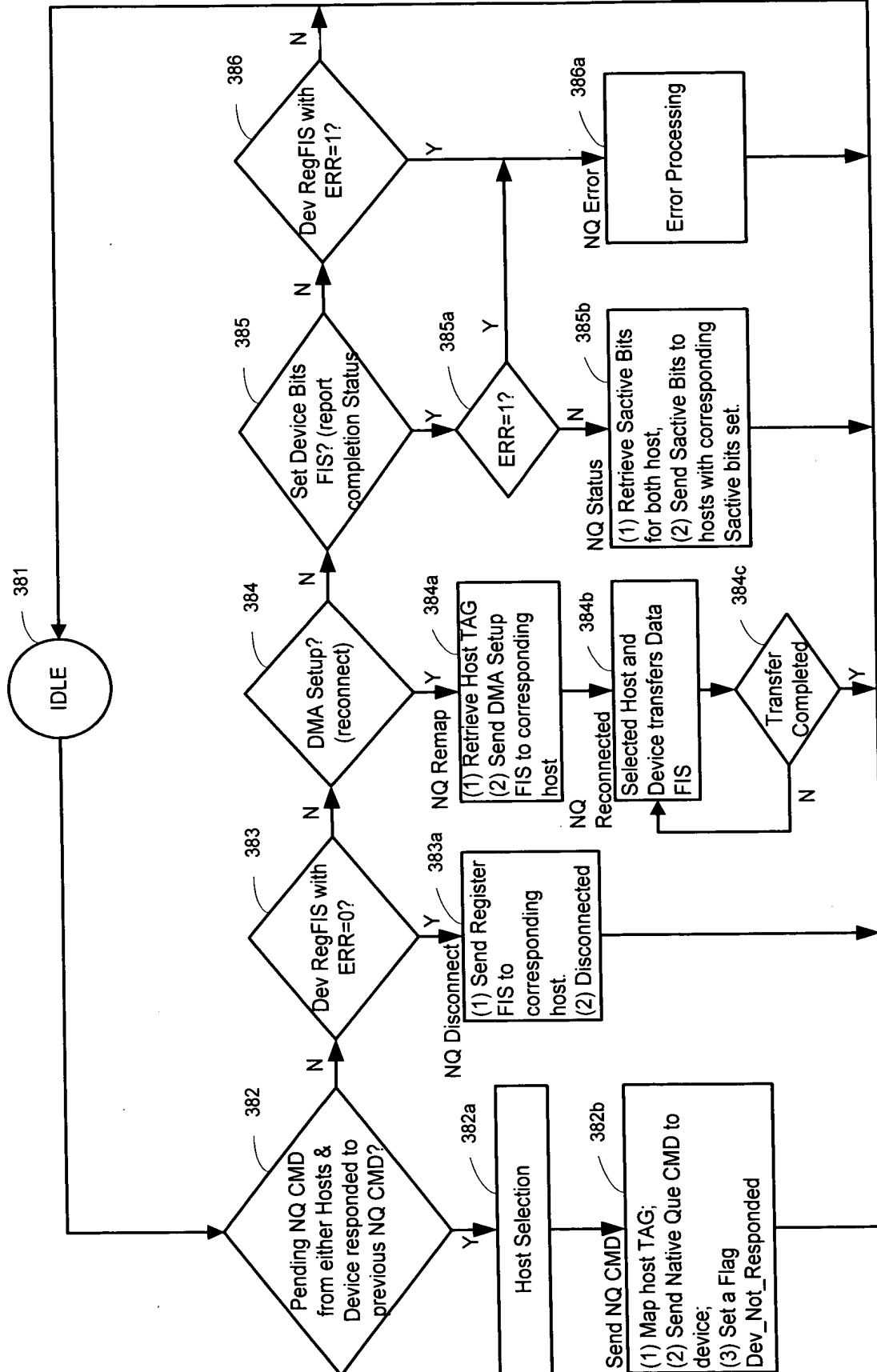


FIG. 8b

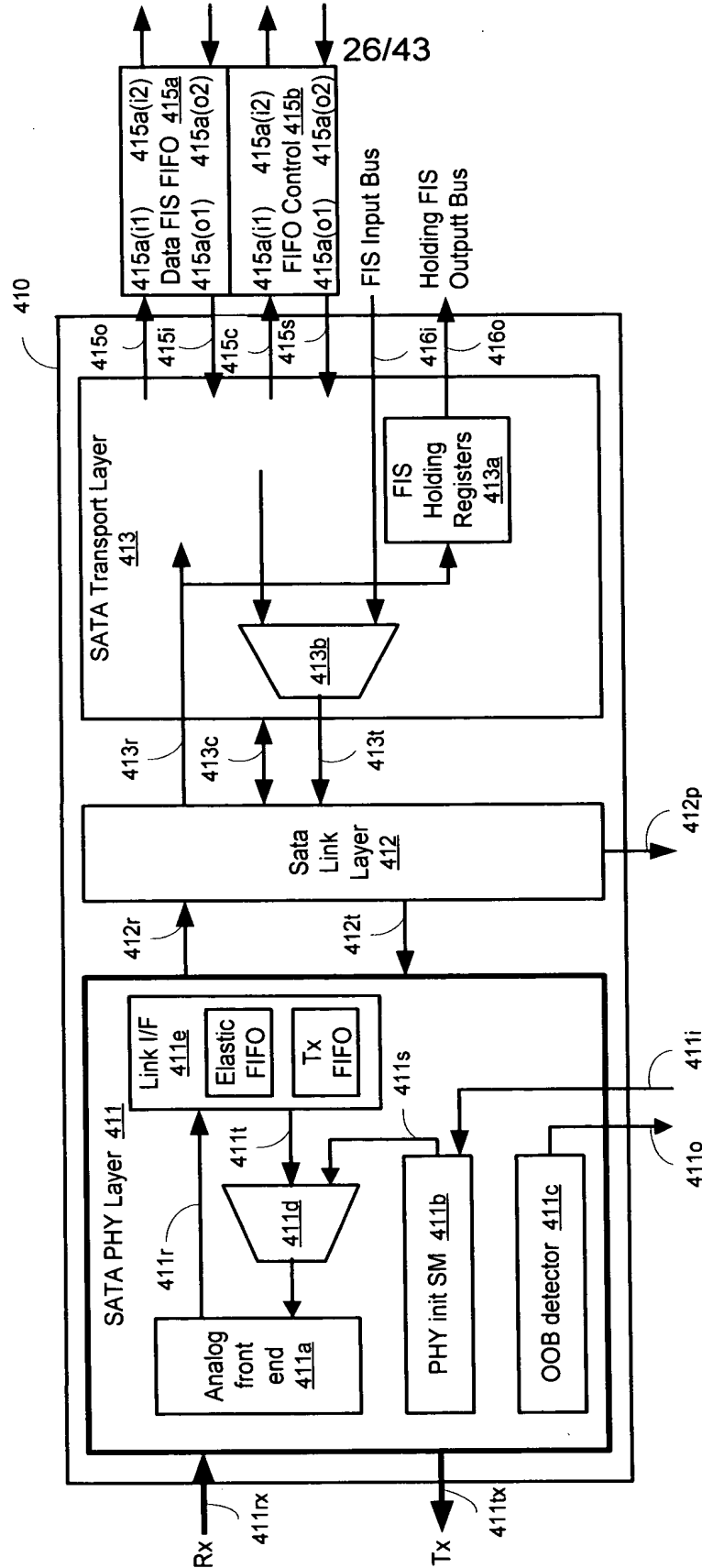
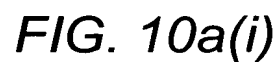


FIG. 9

FIG. 10a



28/43

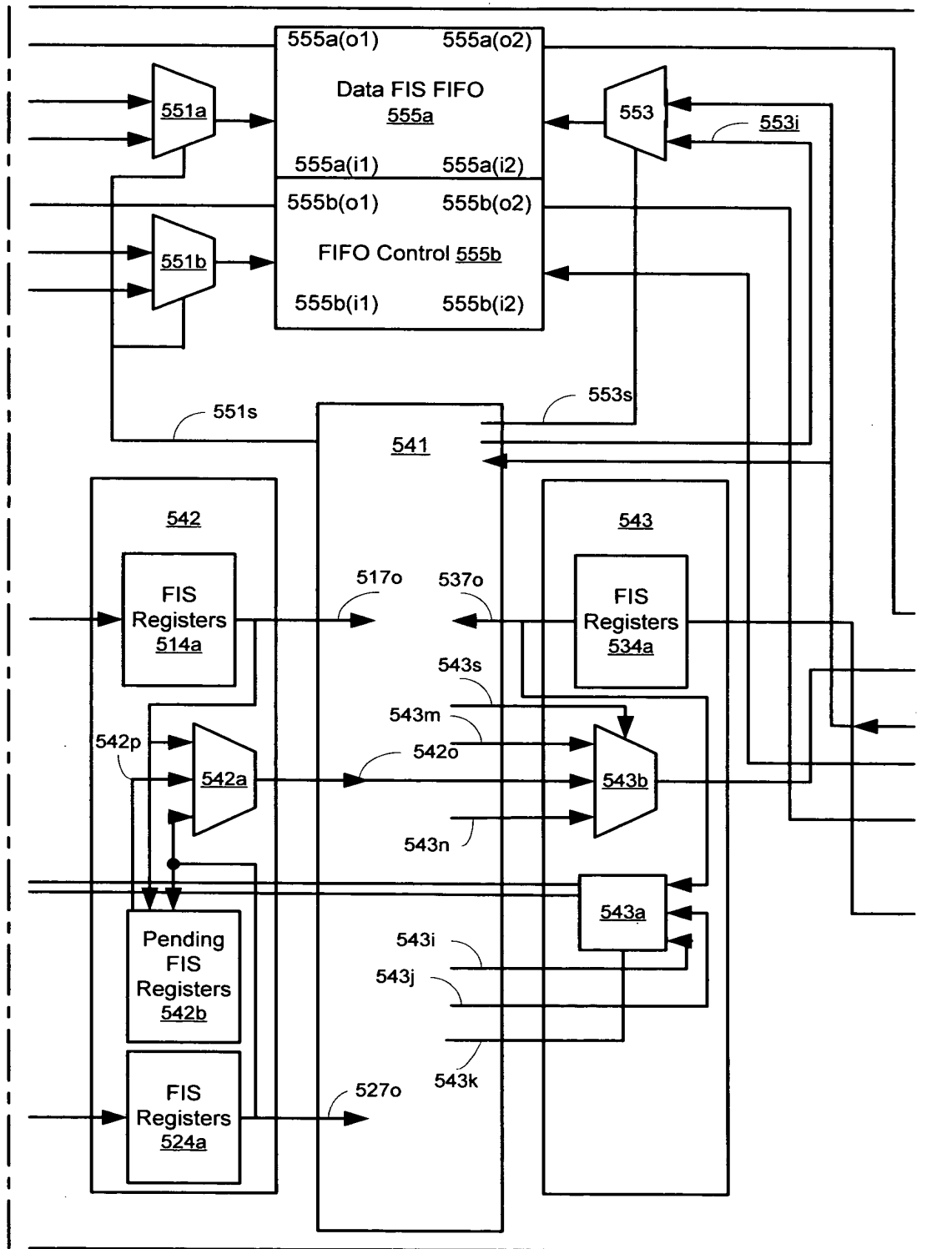


FIG. 10a(ii)

29/43

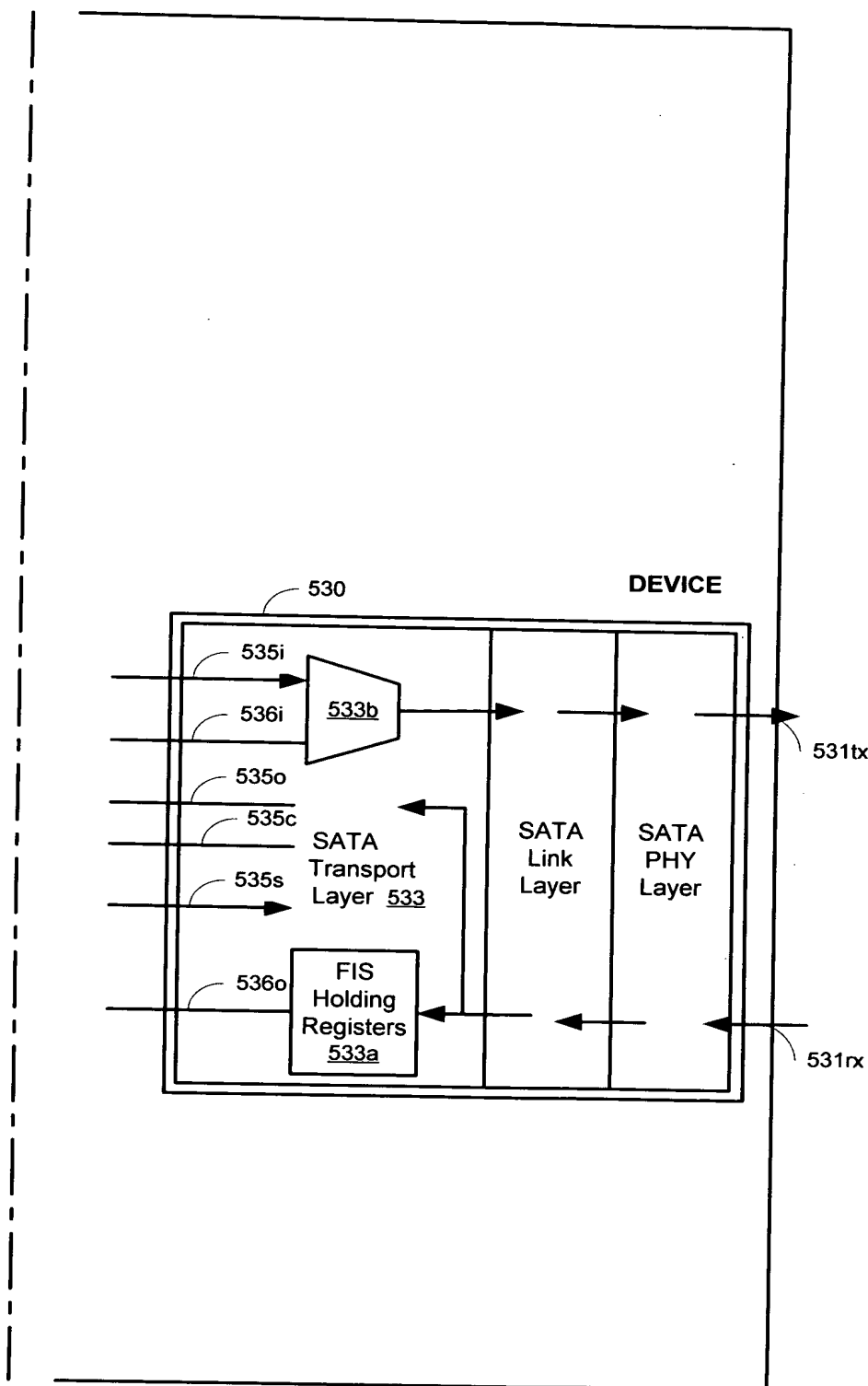


FIG. 10a(iii)

30/43

FIG. 10b(i)	FIG. 10b(ii)	FIG. 10b(iii)
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Key to

FIG. 10b

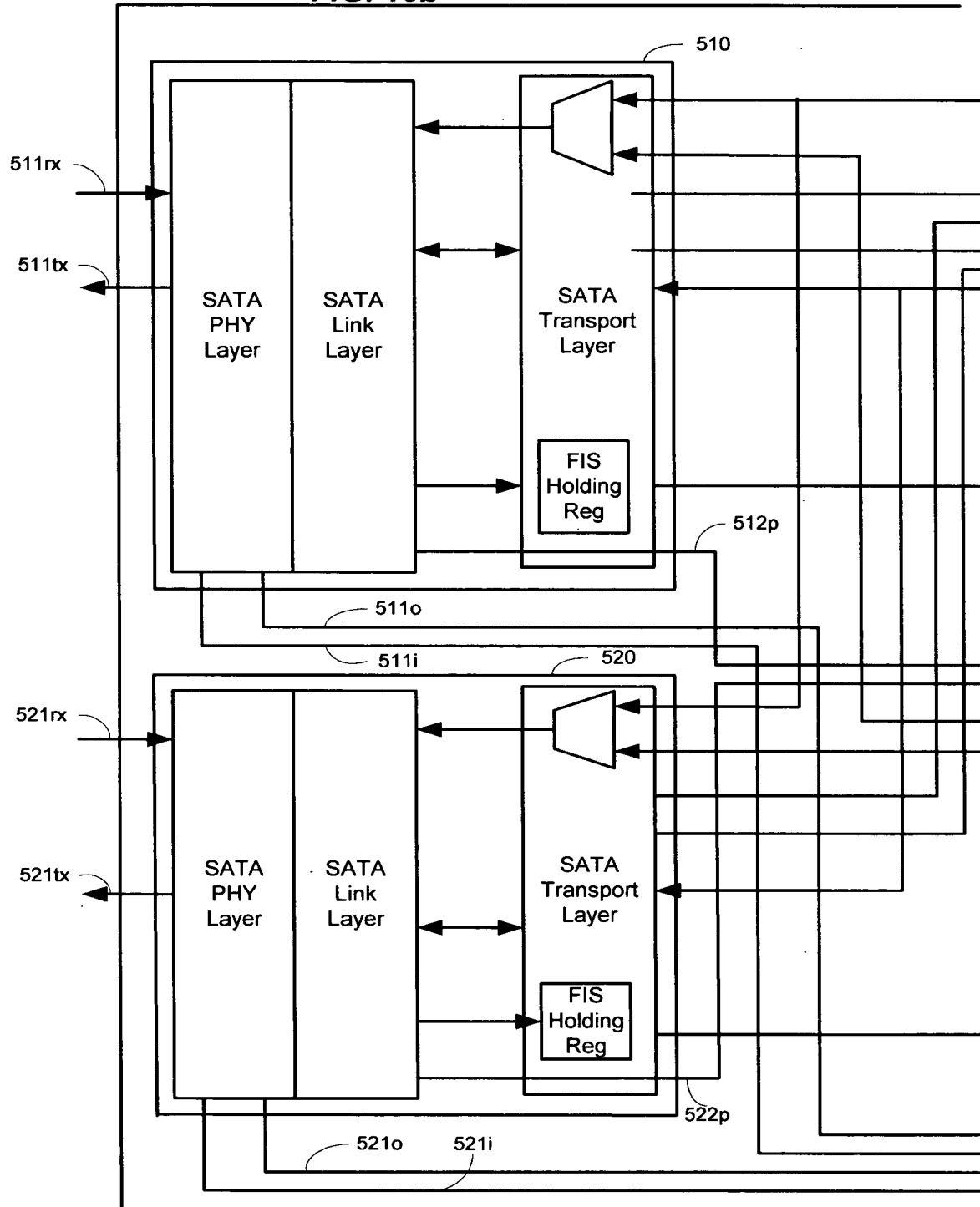


FIG. 10b(i)

31/43

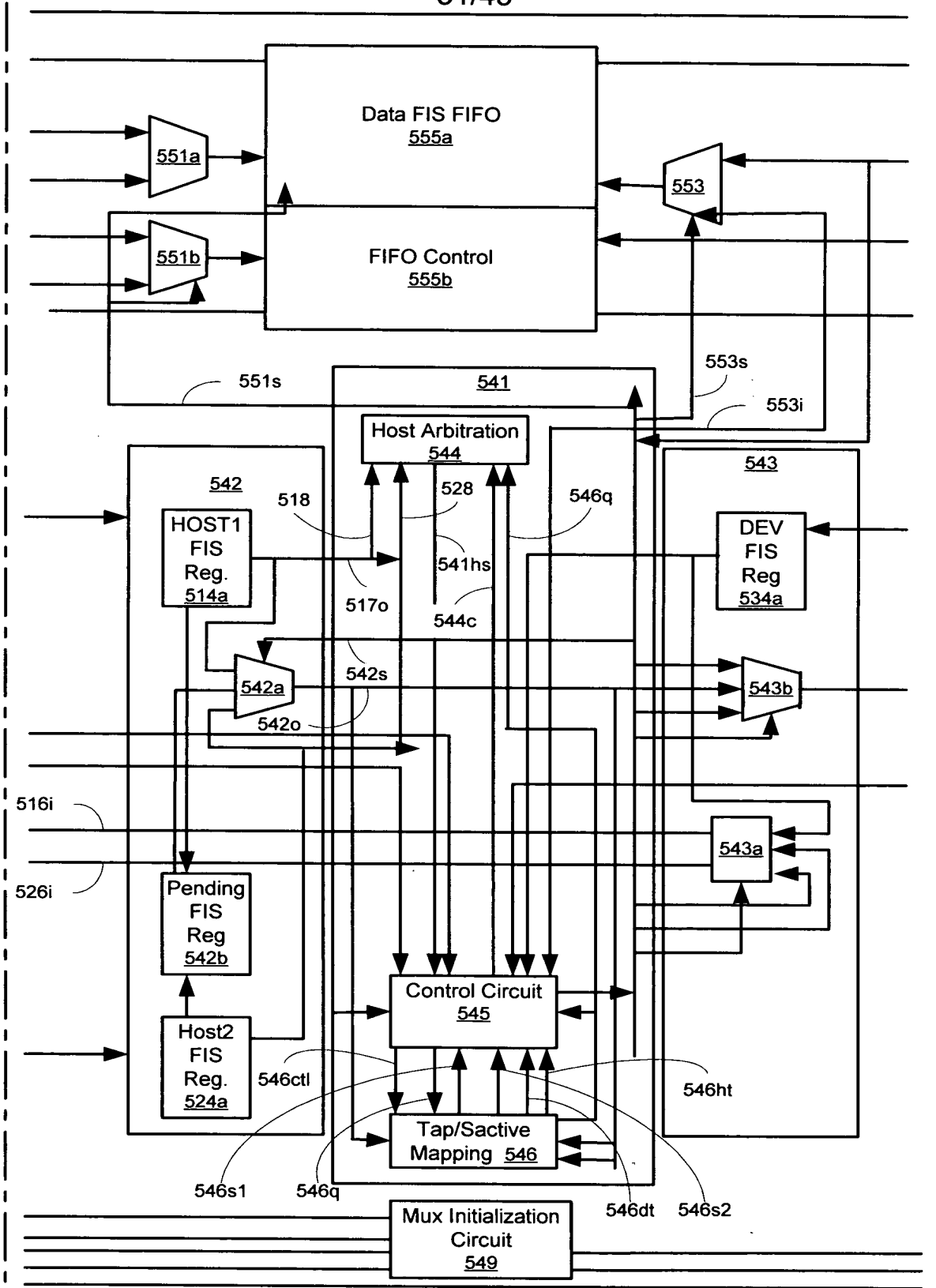


FIG. 10b(ii)

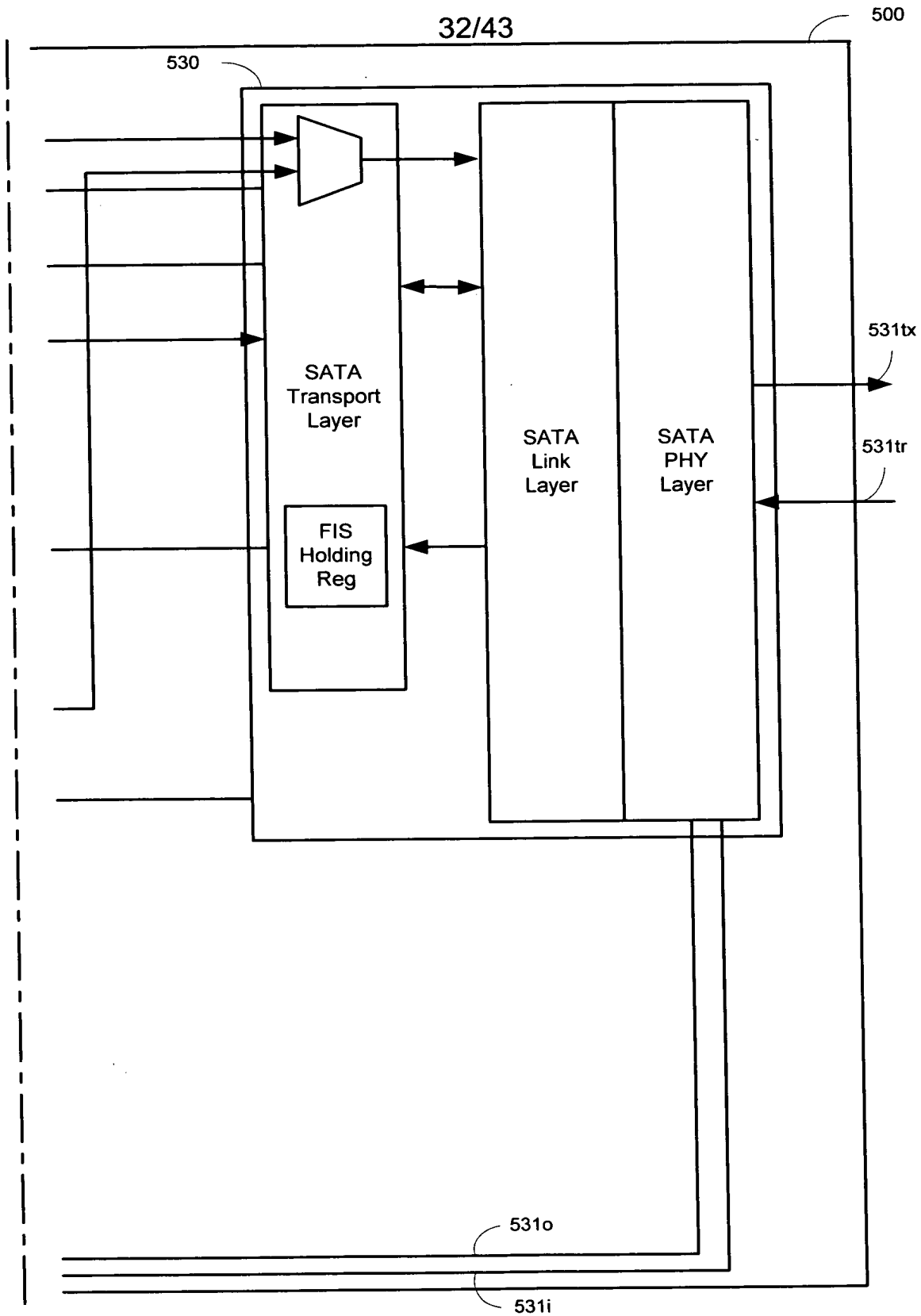


FIG. 10b(iii)

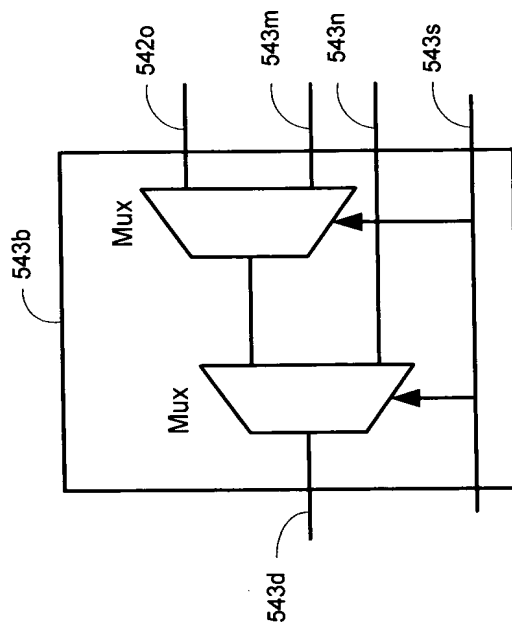
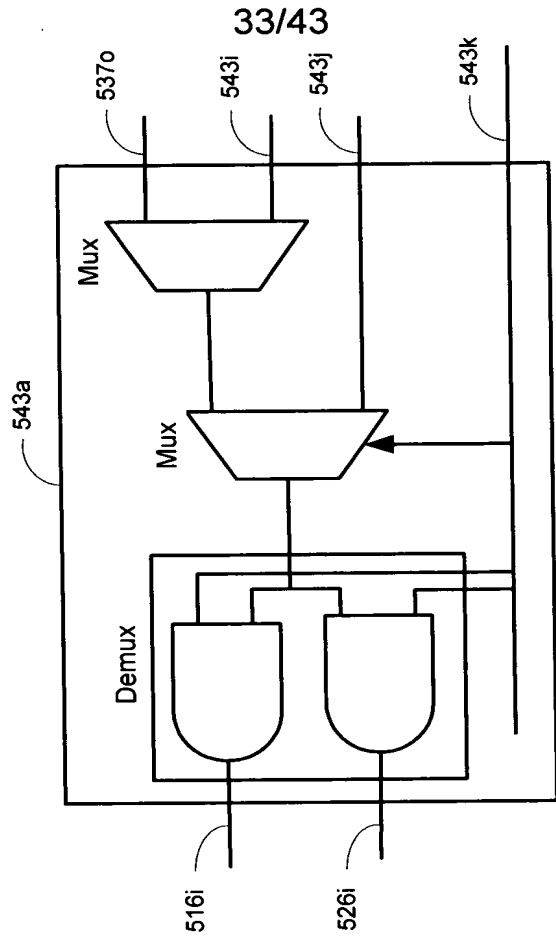
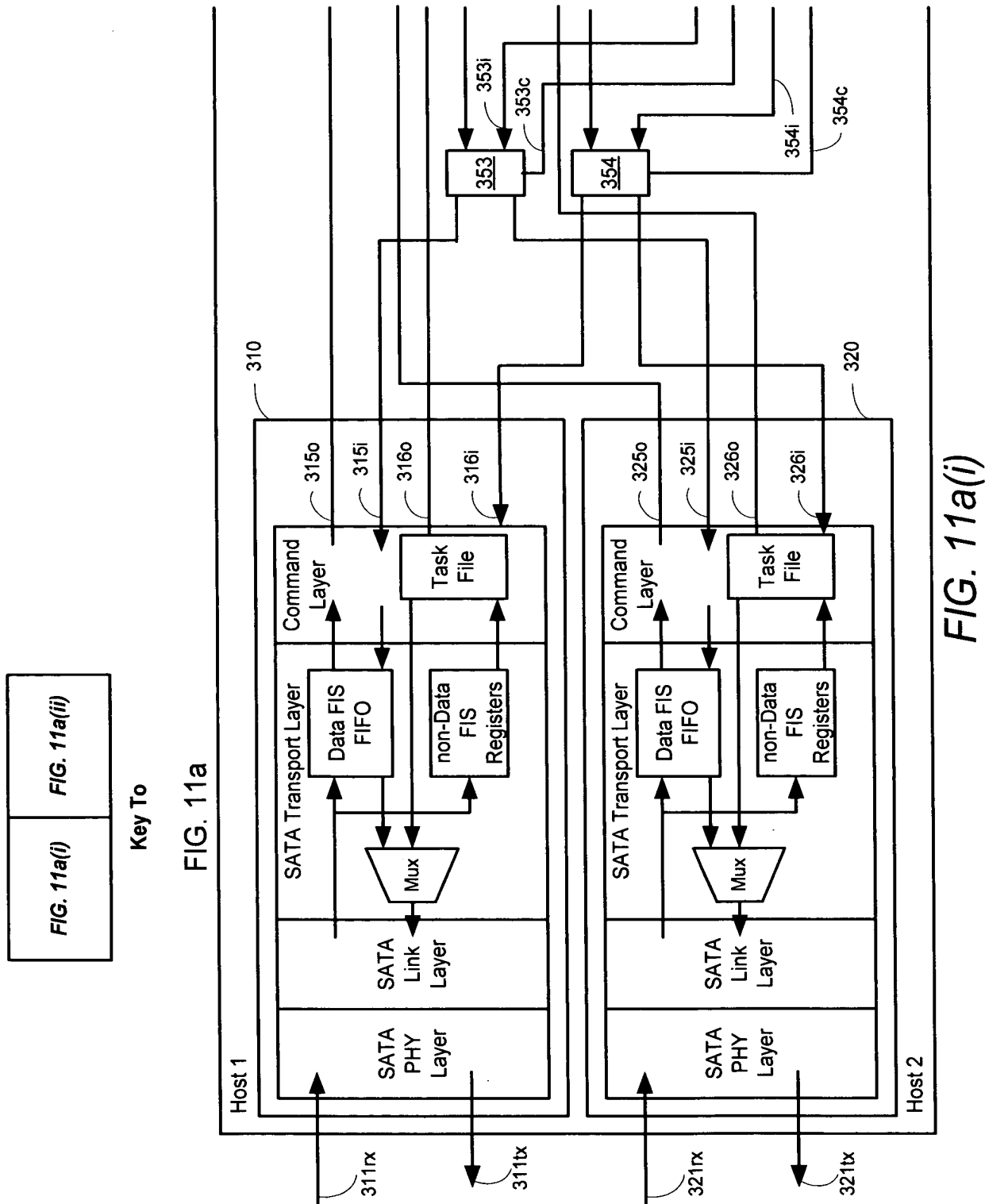


FIG. 10c



35/43

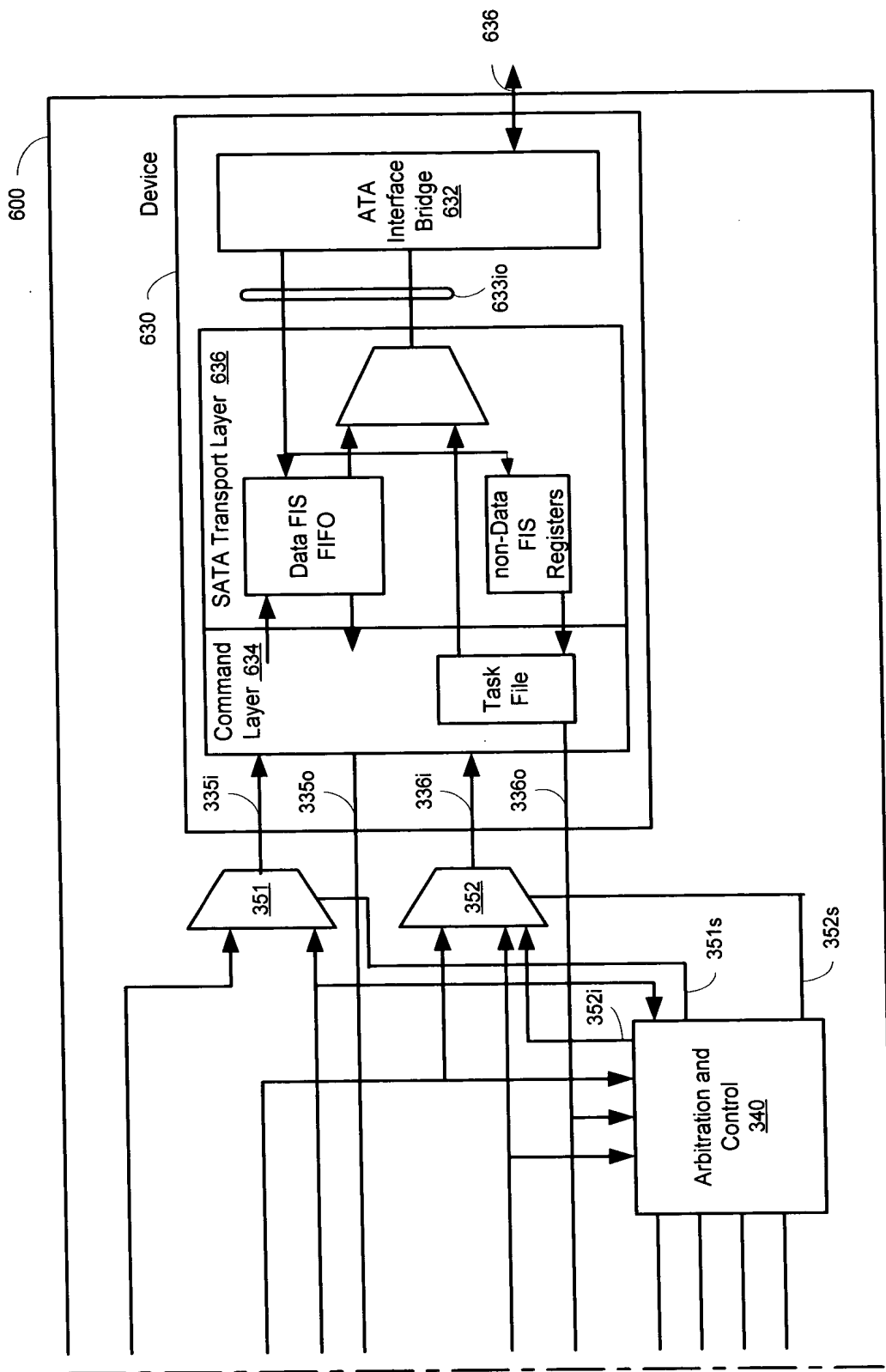


FIG. 11a(ii)

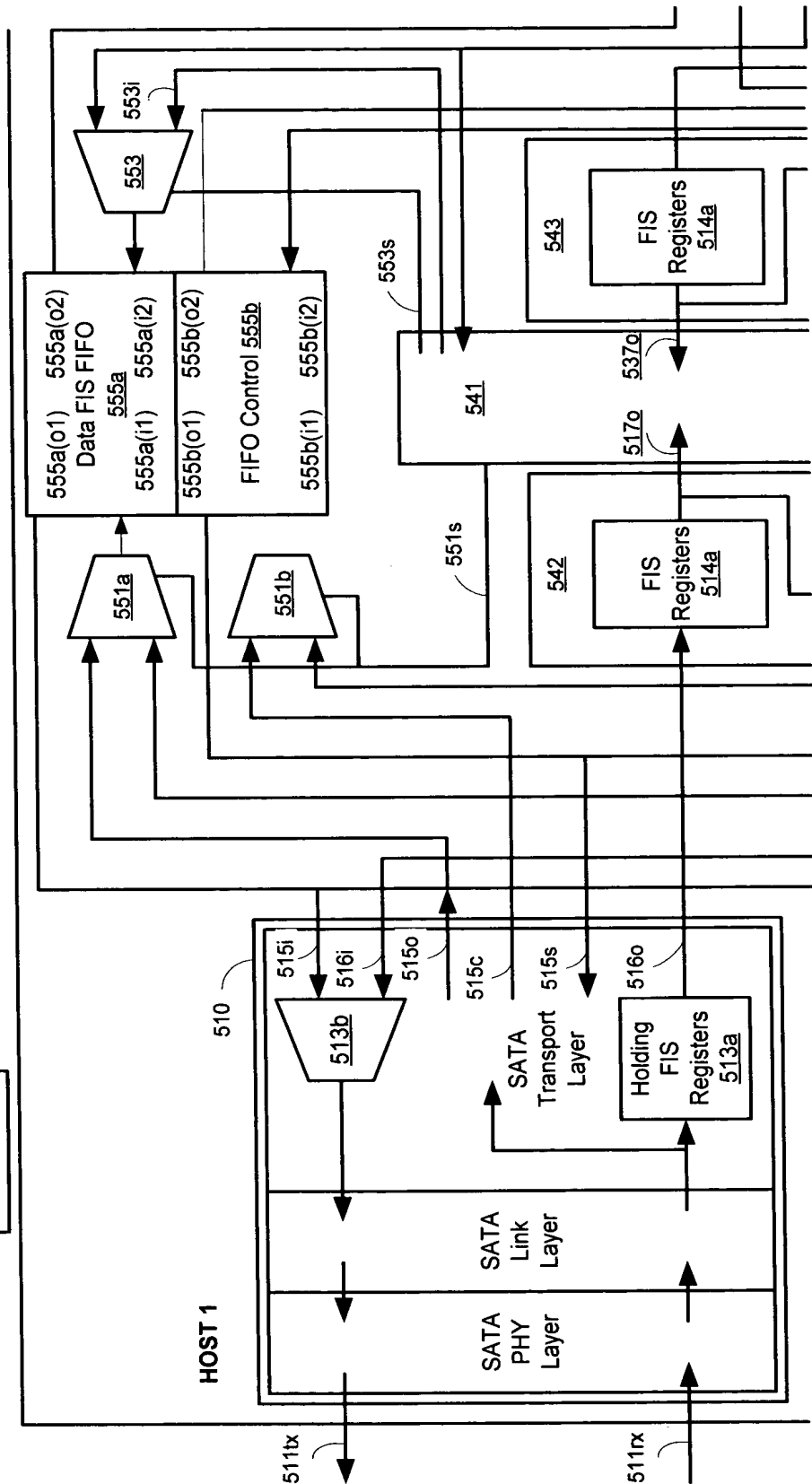
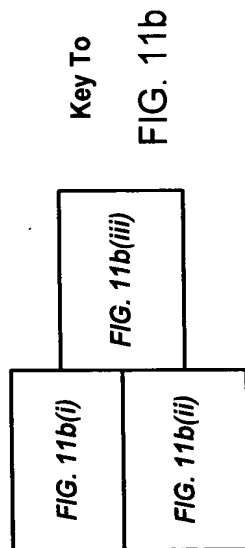


FIG. 11b(i)

37/43

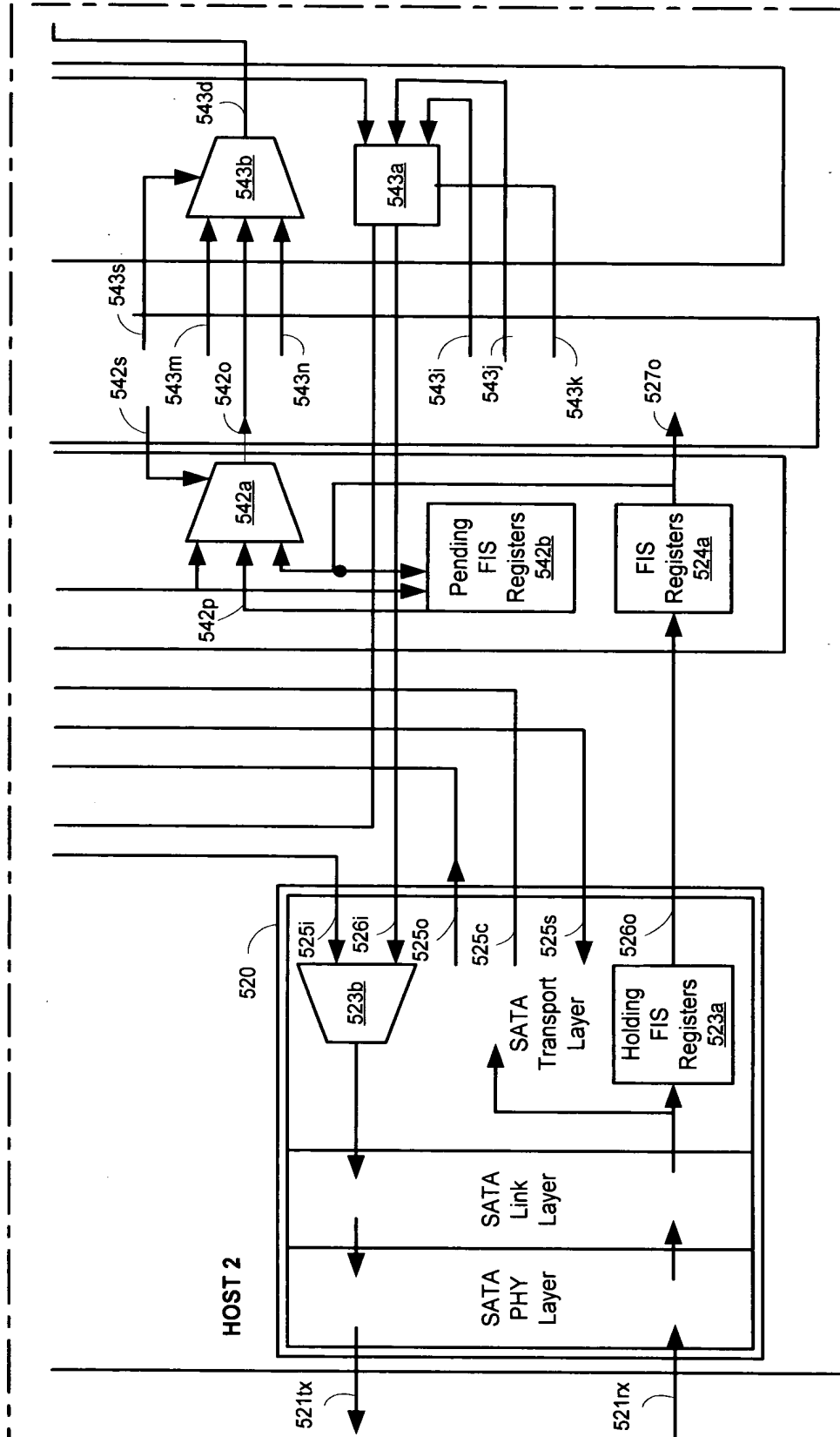


FIG. 11b(ii)

38/43

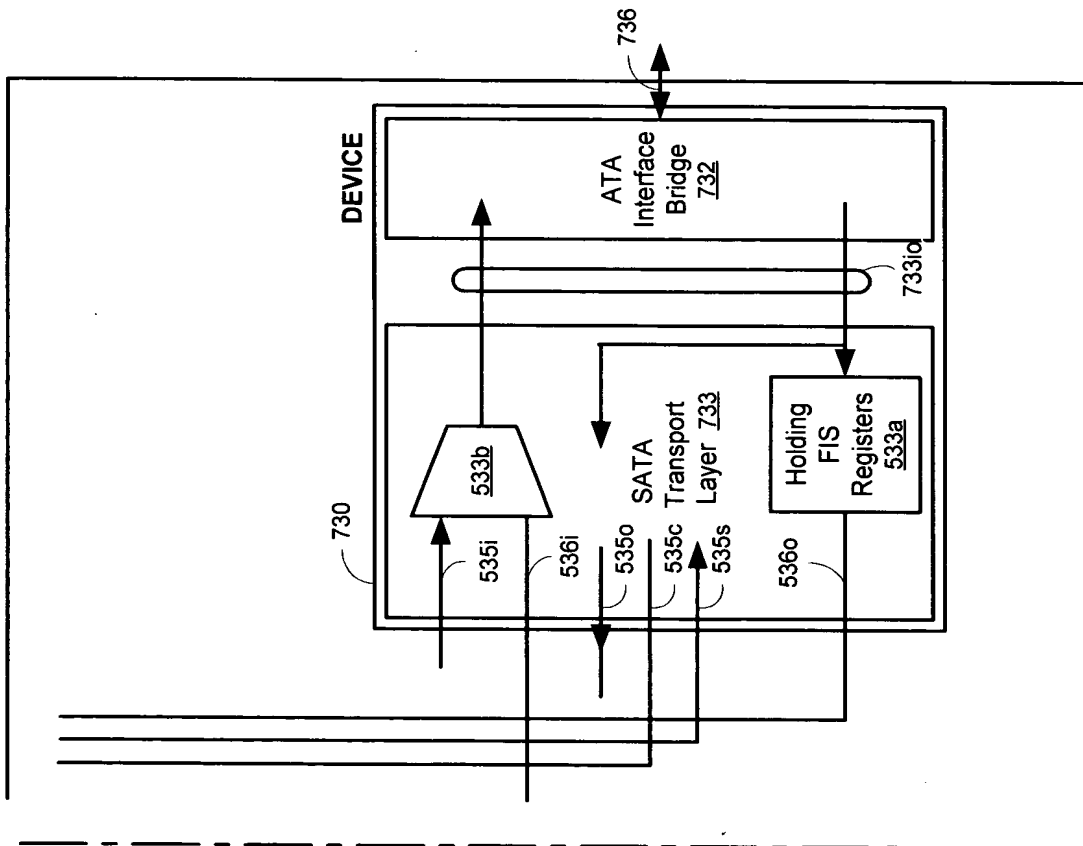


FIG. 11b(iii)

39/43

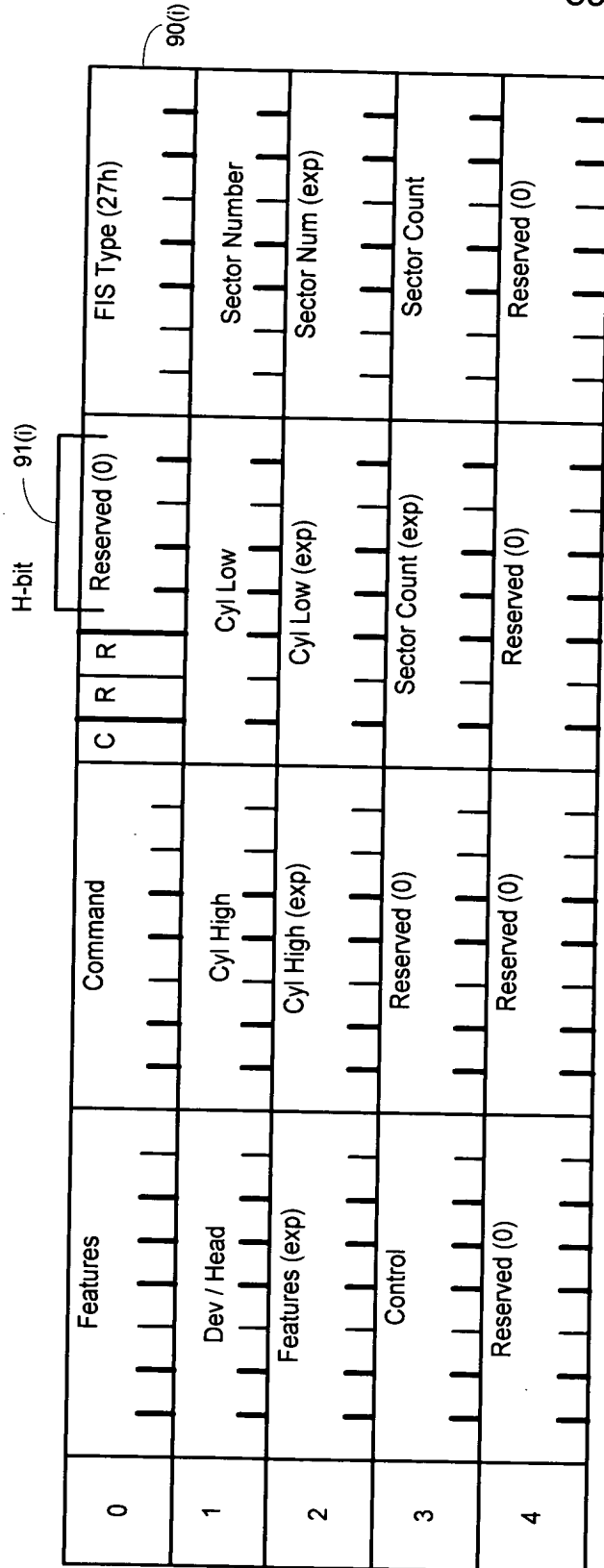


FIG. 12(i) Register FIS Host to Device

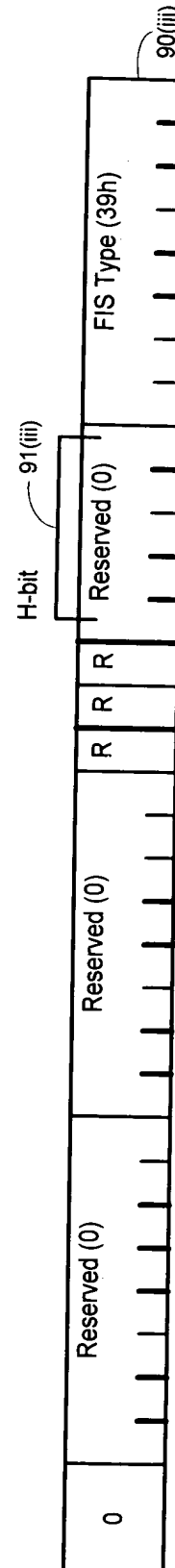


FIG. 12(iii) DMA Activate FIS, Device to Host

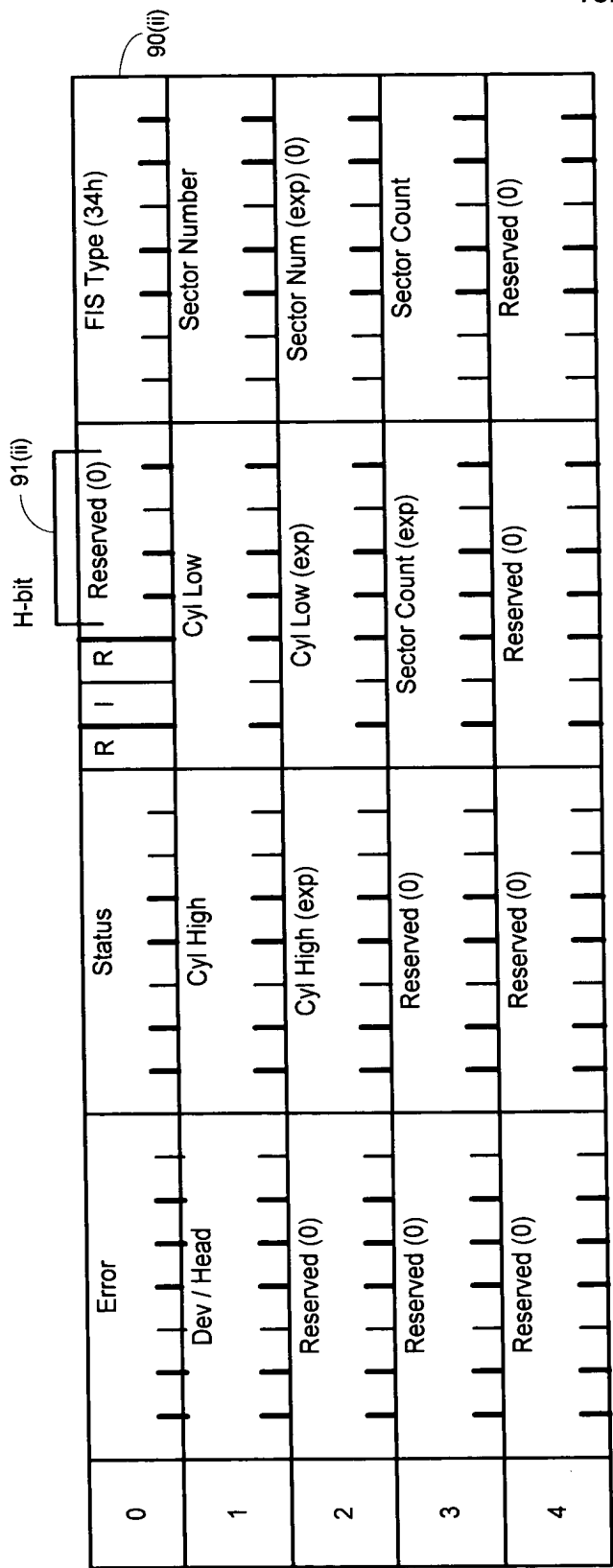


FIG. 12(ii) Register FIS Device to Host

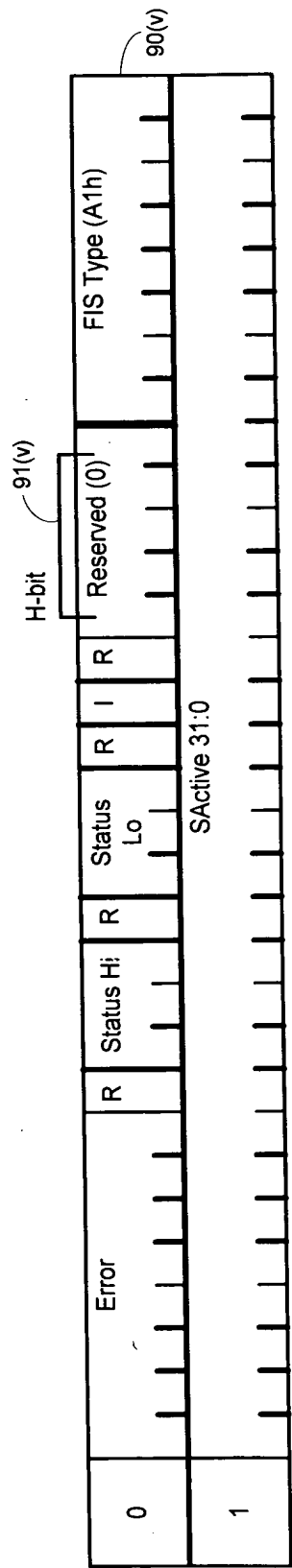


FIG. 12(v) Set Device Bits FIS

41/43

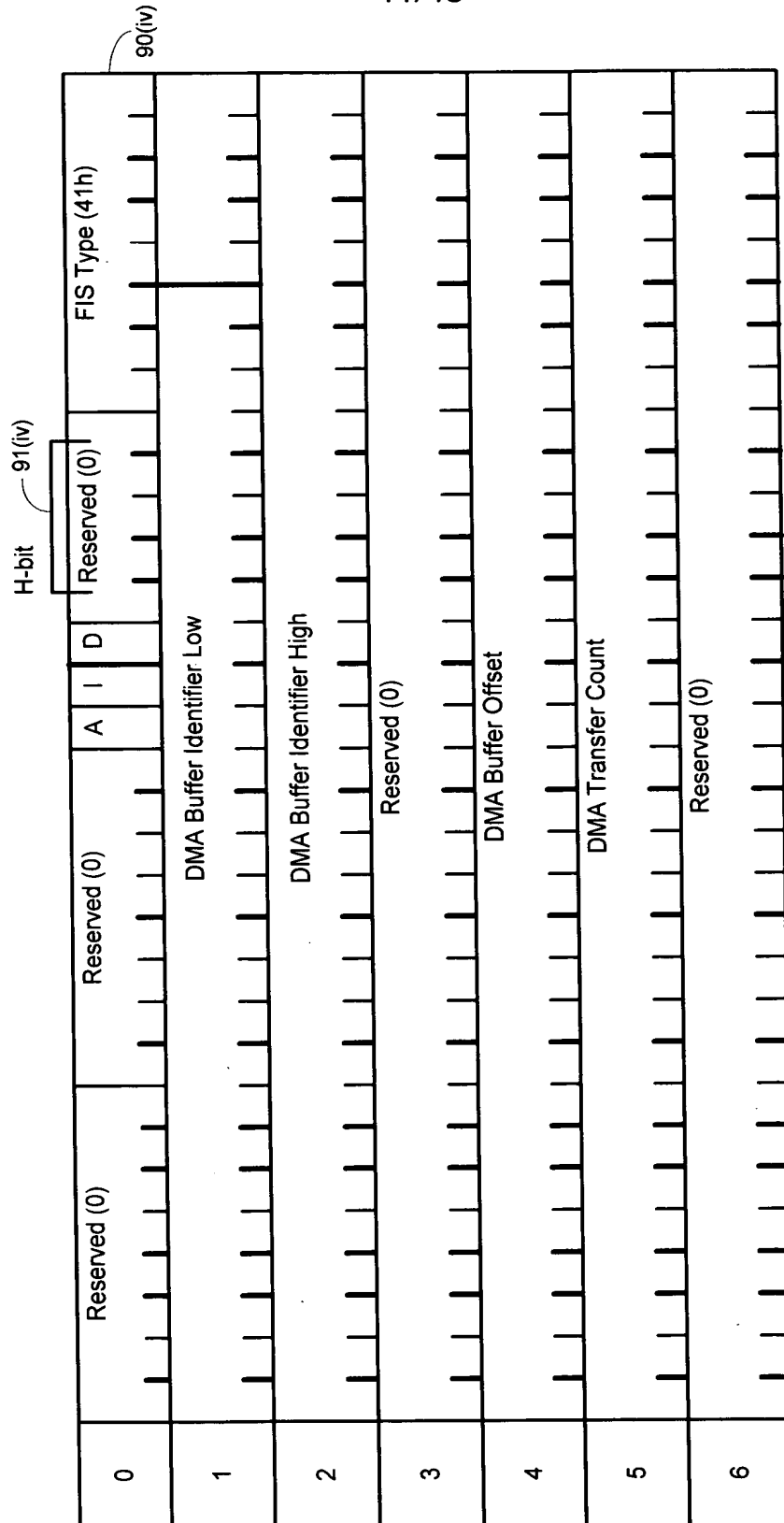


FIG. 12(iv) DMA Setup FIS

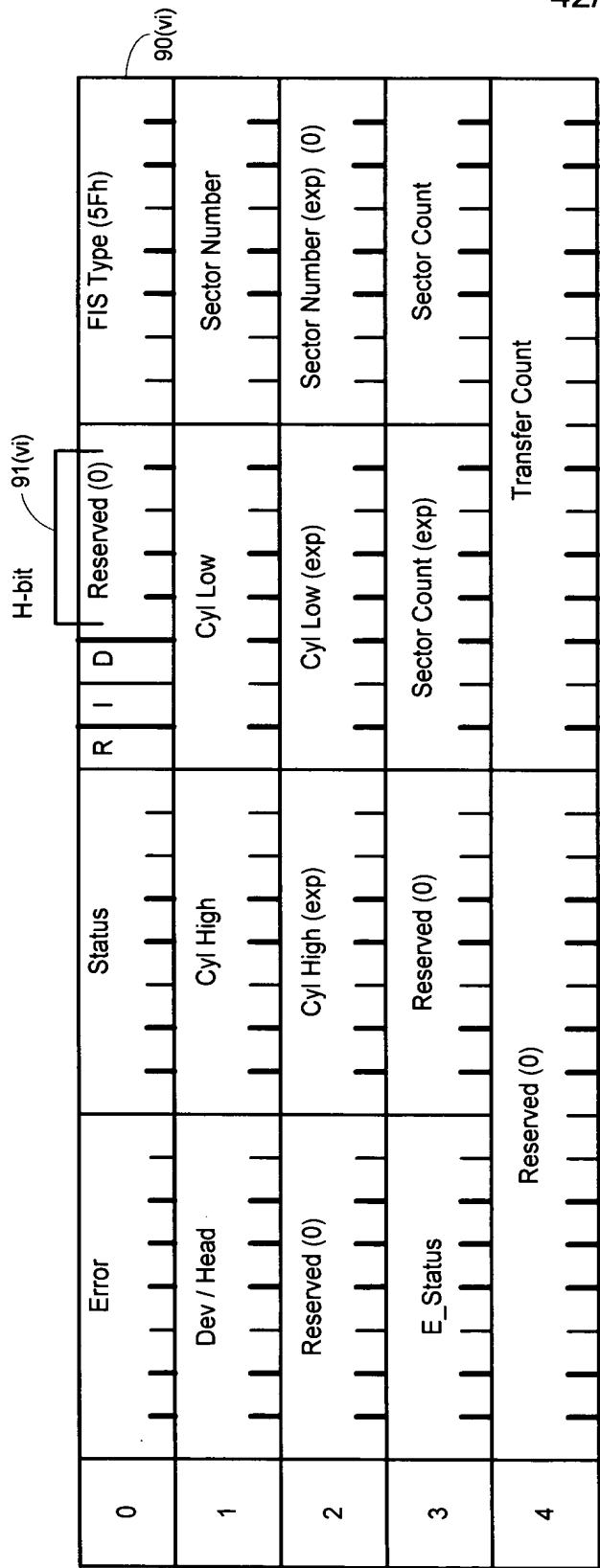


FIG. 12(vi) PIO Setup FIS

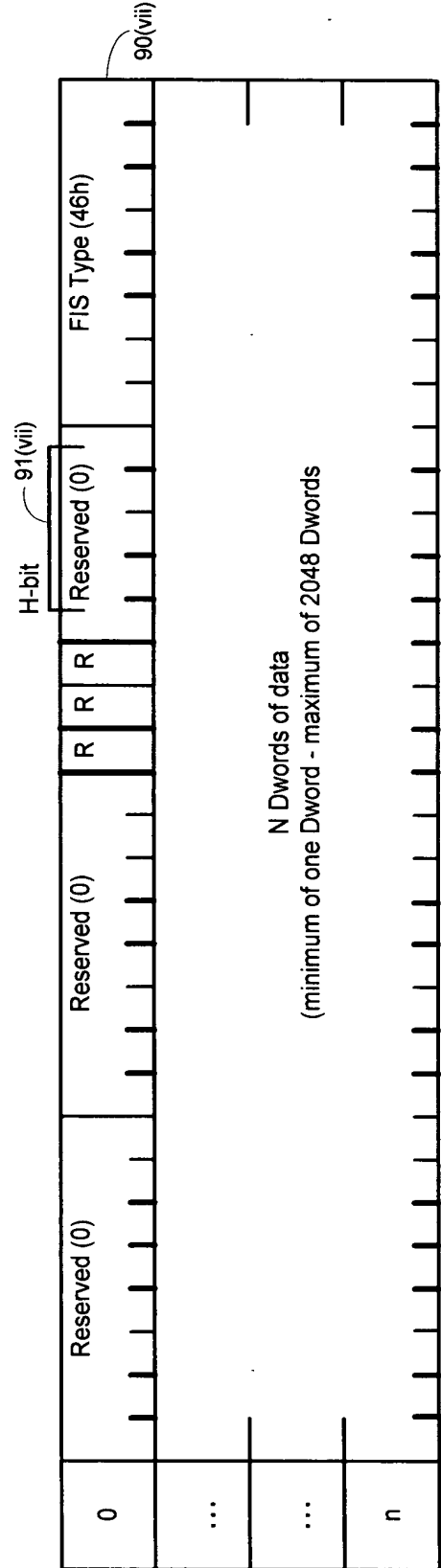


FIG. 12(vii) Data FIS

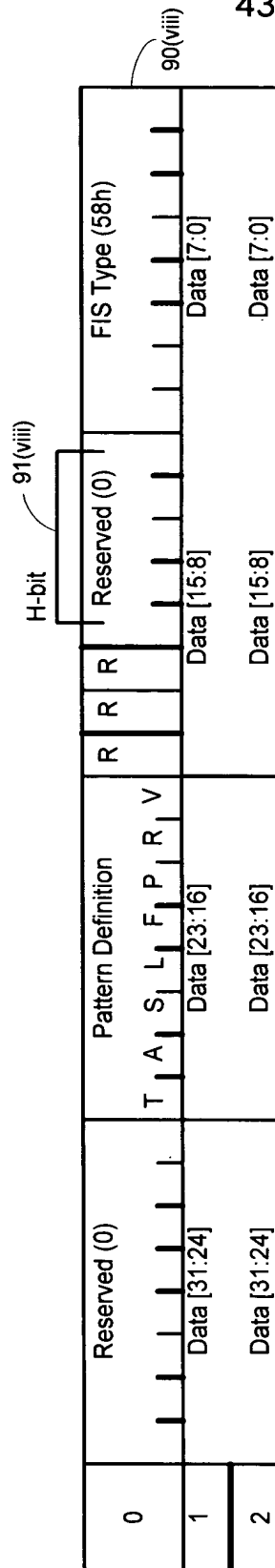


FIG. 12(viii) BIST Activate FIS